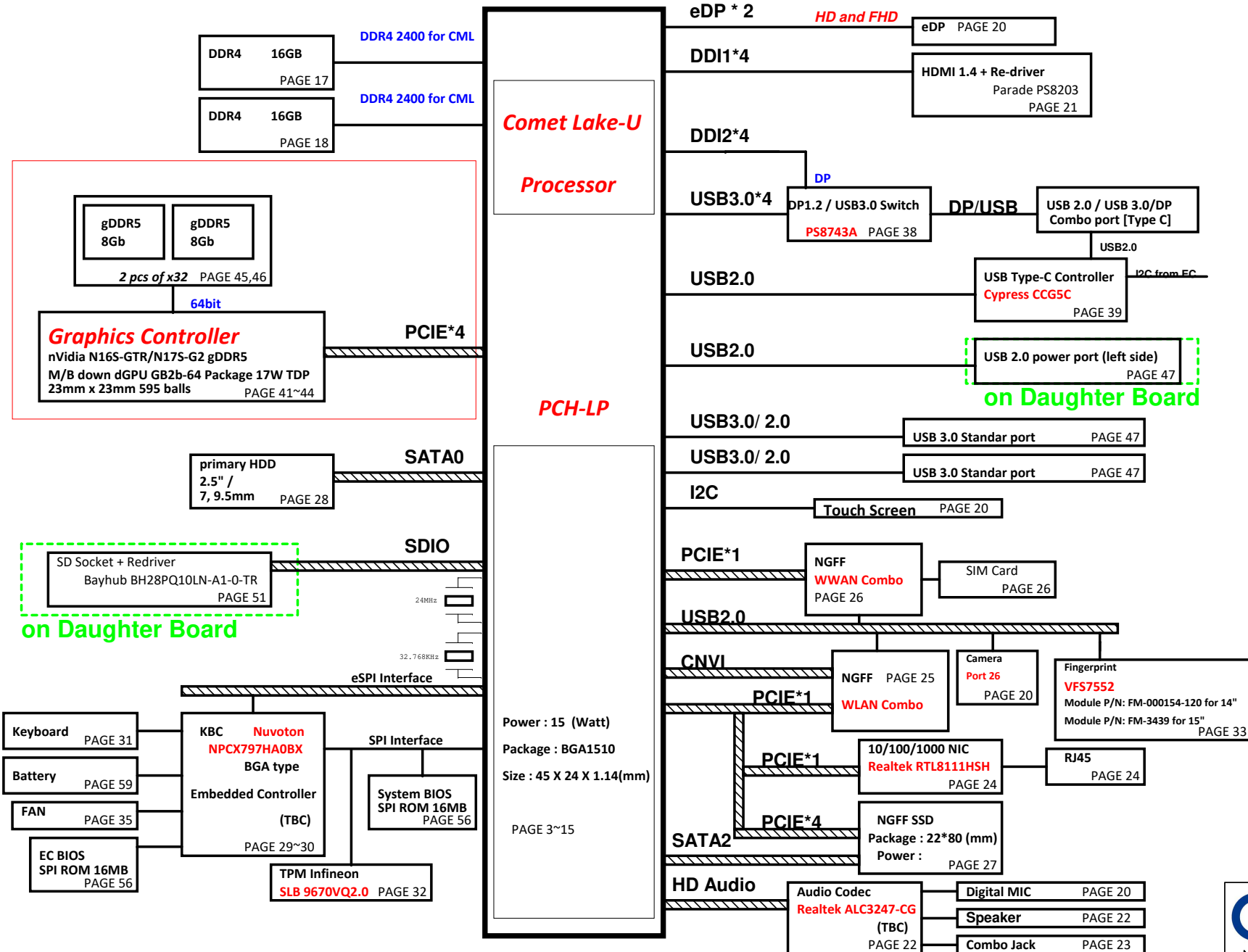
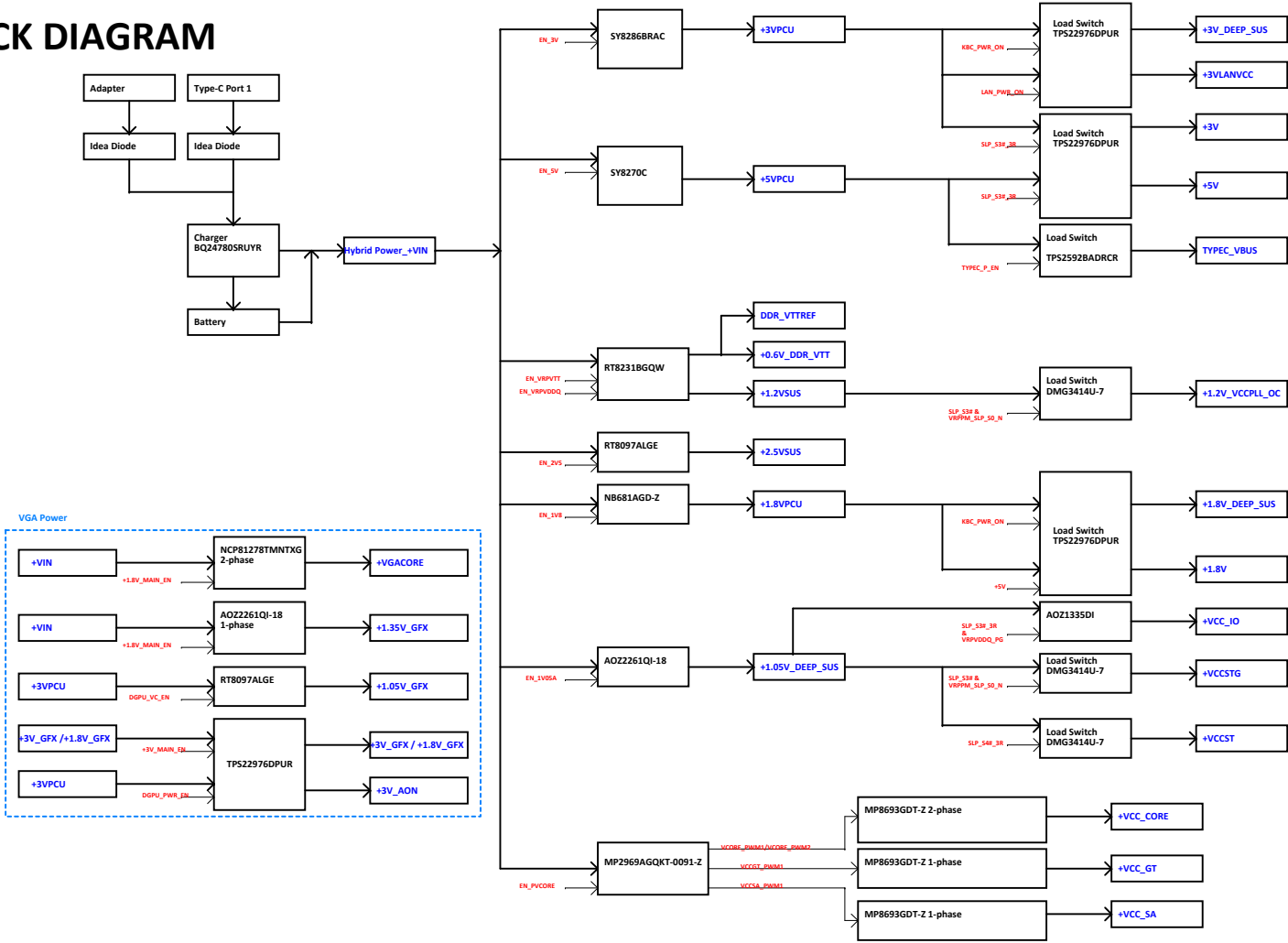


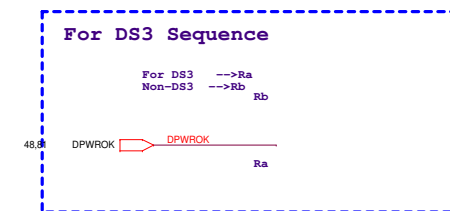
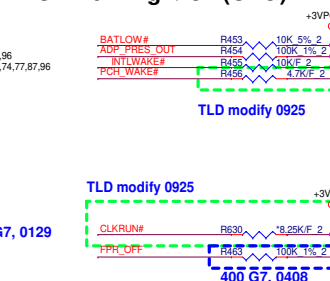
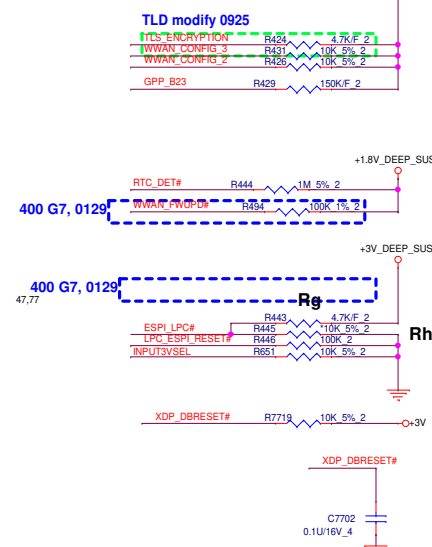
S400 G7 CML (UMA/DIS) Block Diagram

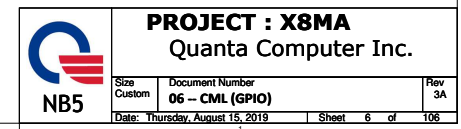


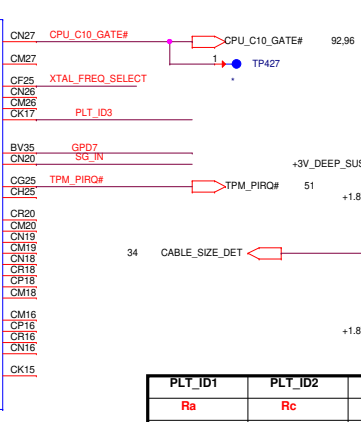
POWER BLOCK DIAGRAM





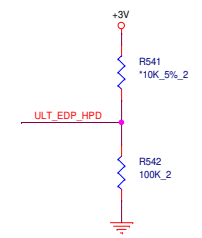
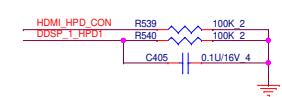
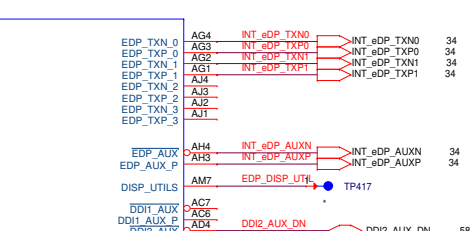
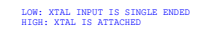
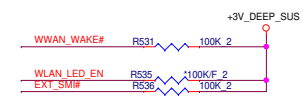
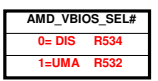




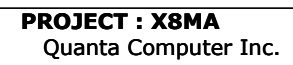


SG_IN	
DIS=1	R521 (Default)
UMA=0	R522

XTAL_FREQ_SELECT	
LOW	38.4/19.2MHZ
HIGH	24MHZ(default)

[illegible]

1 of 20

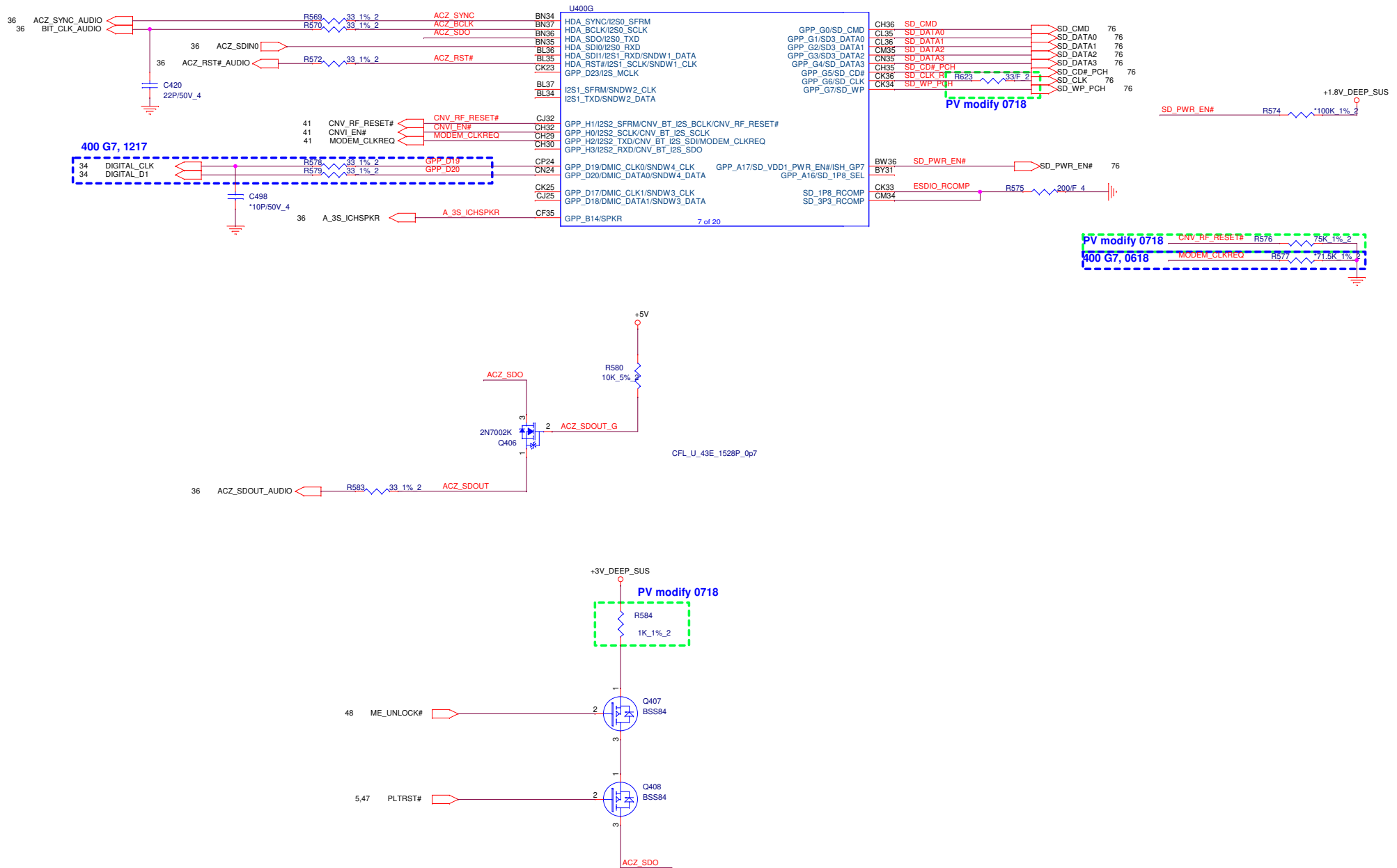


Size Custom	Document Number 07 – CML (eDP/DDI/Board ID)	Rev 3A
Date: Thursday, August 15, 2019		Sheet 7 of 106

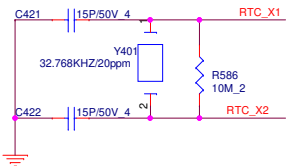


Size Custom	Document Number 08 – CML (DDR3-A/B I/F)	Rev 3A
Date: Thursday, August 15, 2019	Sheet 8 of	106

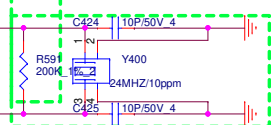




RTC Clock 32.768KHz

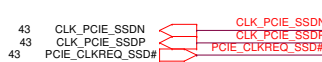


PV Modify 0727



TLD Modify 0715

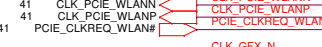
SSD



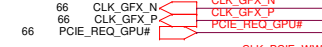
Cardreader



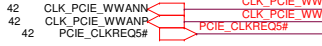
WLAN



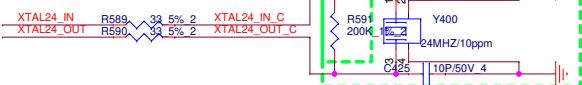
dGPU



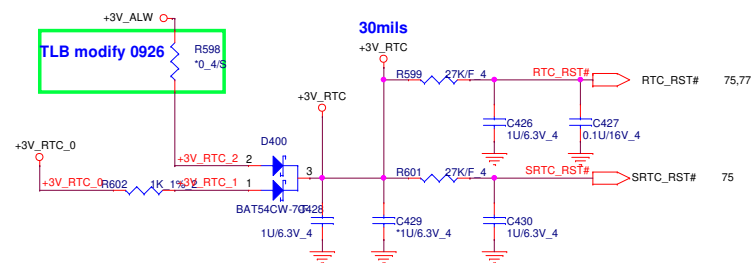
WWAN



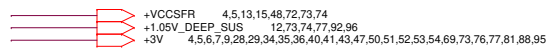
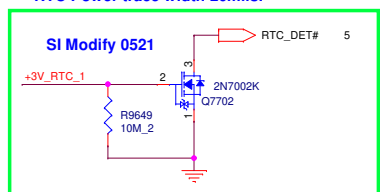
SI Modify 0530



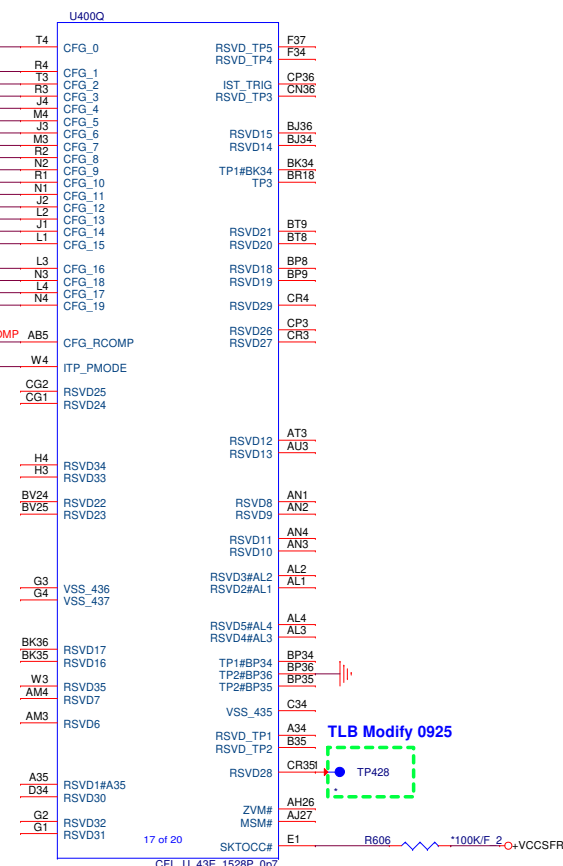
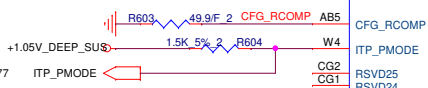
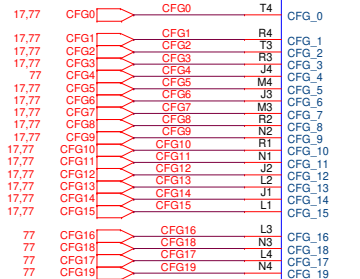
RTC Circuitry(RTC)



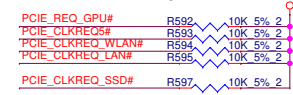
RTC Power trace width 20mils.



CFG0-19 need Reserve TP




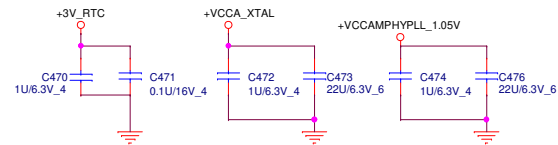
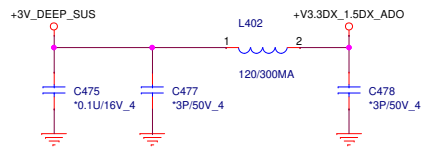
CLK_REQ/Strap Pin(CLG)



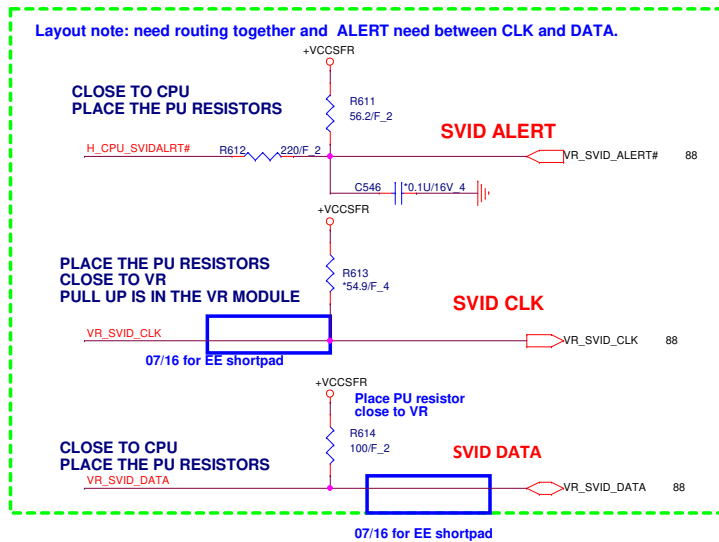
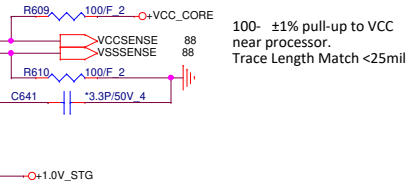
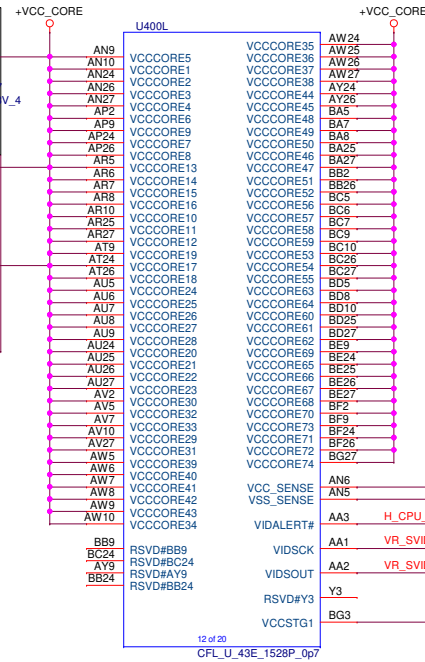
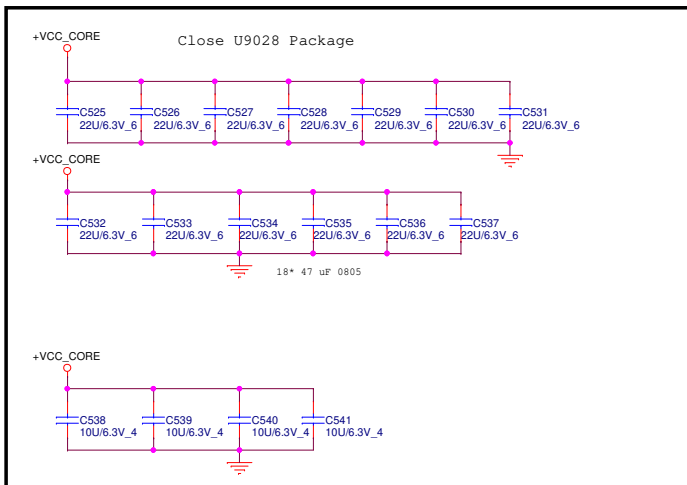
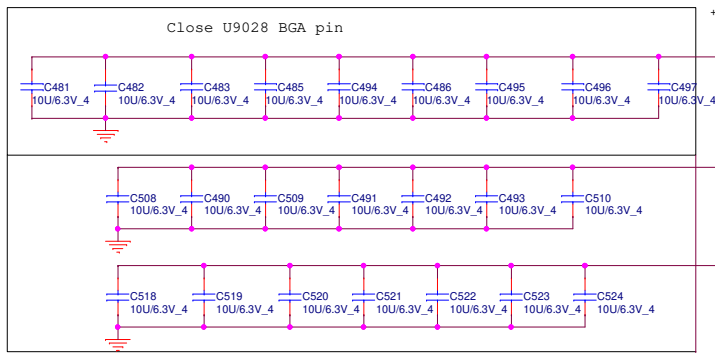
Modify 0925



 NB5	PROJECT : X8MA Quanta Computer Inc.		
	Size Custom	Document Number 11 -- CML (CLK/RSV/RTC)	Rev 3A
	Date: Thursday, August 15, 2019 Sheet 11 of 106		

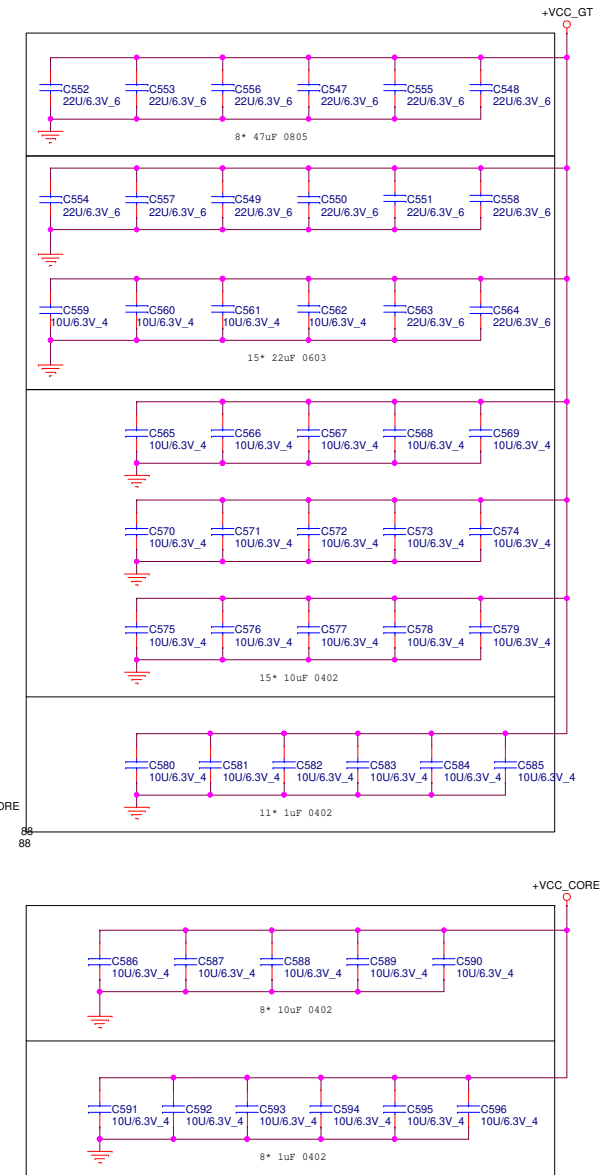
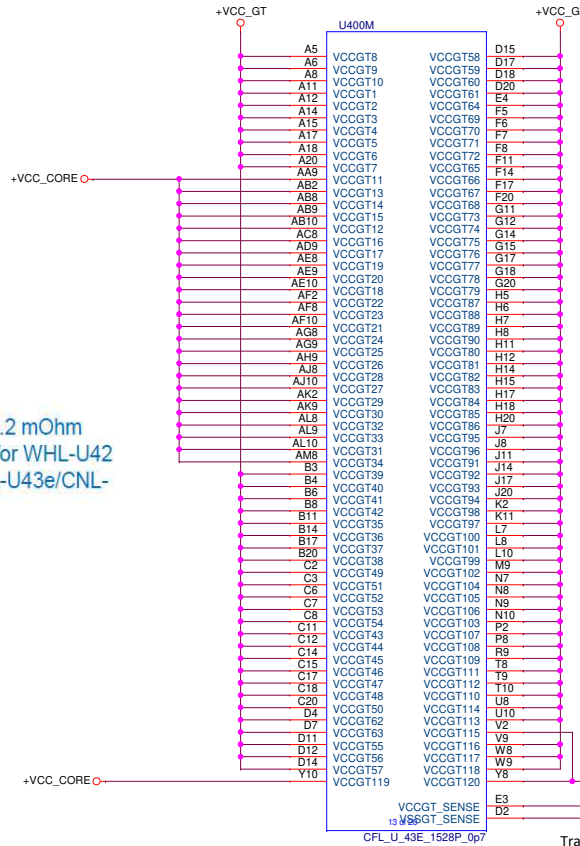


→	+3V_DEEP_SUS	5,6,7,8,9,10,33,40,41,42,47,56,74,77,81,82,95
→	+3VPU	5,7,33,34,36,41,42,47,48,50,54,56,58,61,73,74,75,77,80,81,82,85,86,87,88,92,93,95,105
→	+1.05V_DEEP_SUS	11,73,74,77,92,96
→	+3V	4,5,6,7,9,11,28,29,33,35,36,40,41,43,47,50,51,52,53,54,69,73,76,77,81,88,95
→	+1.8V_DEEP_SUS	5,6,10,41,47,81,95



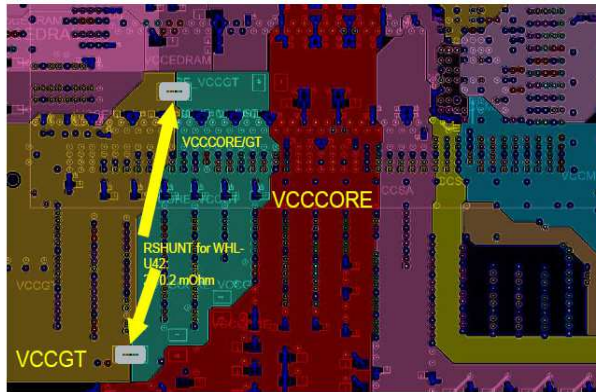
+VCC_CORE 14,72,73,88,89
+VCCSFR 4,5,11,15,48,72,73,74
+1.0V_STG 4,15

400 G7, 0417



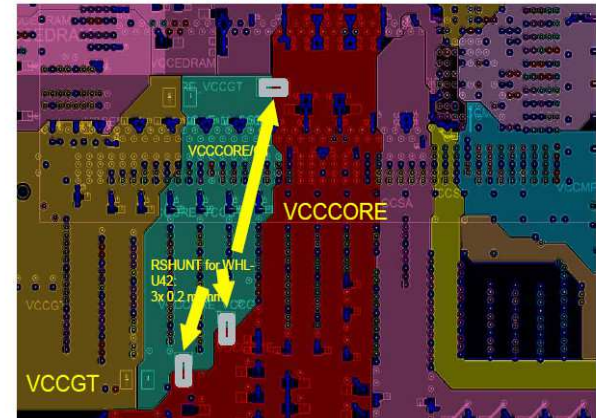
Routing guideline for RSHUNT placement for WHL ES1, CFL43e and CNLU22

Place 2x 0.2 mOhm RSHUNT for WHL-U42 (ES1)/CFL-U43e/CNL-U22

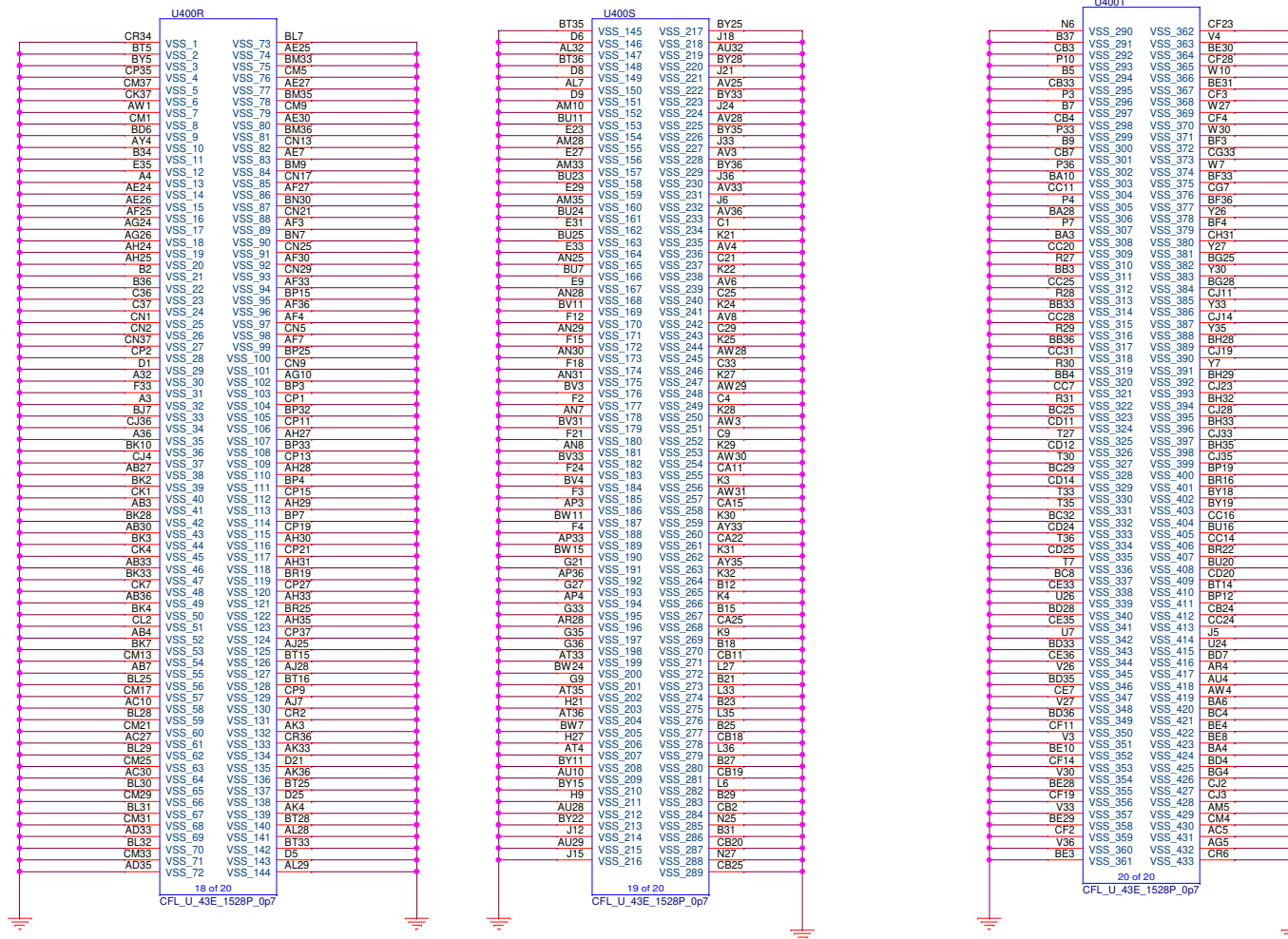


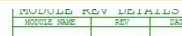
Routing guideline for RSHUNT placement for WHL ES2

Place 3x 0.2 mOhm RSHUNT for WHL-U42 (ES2)







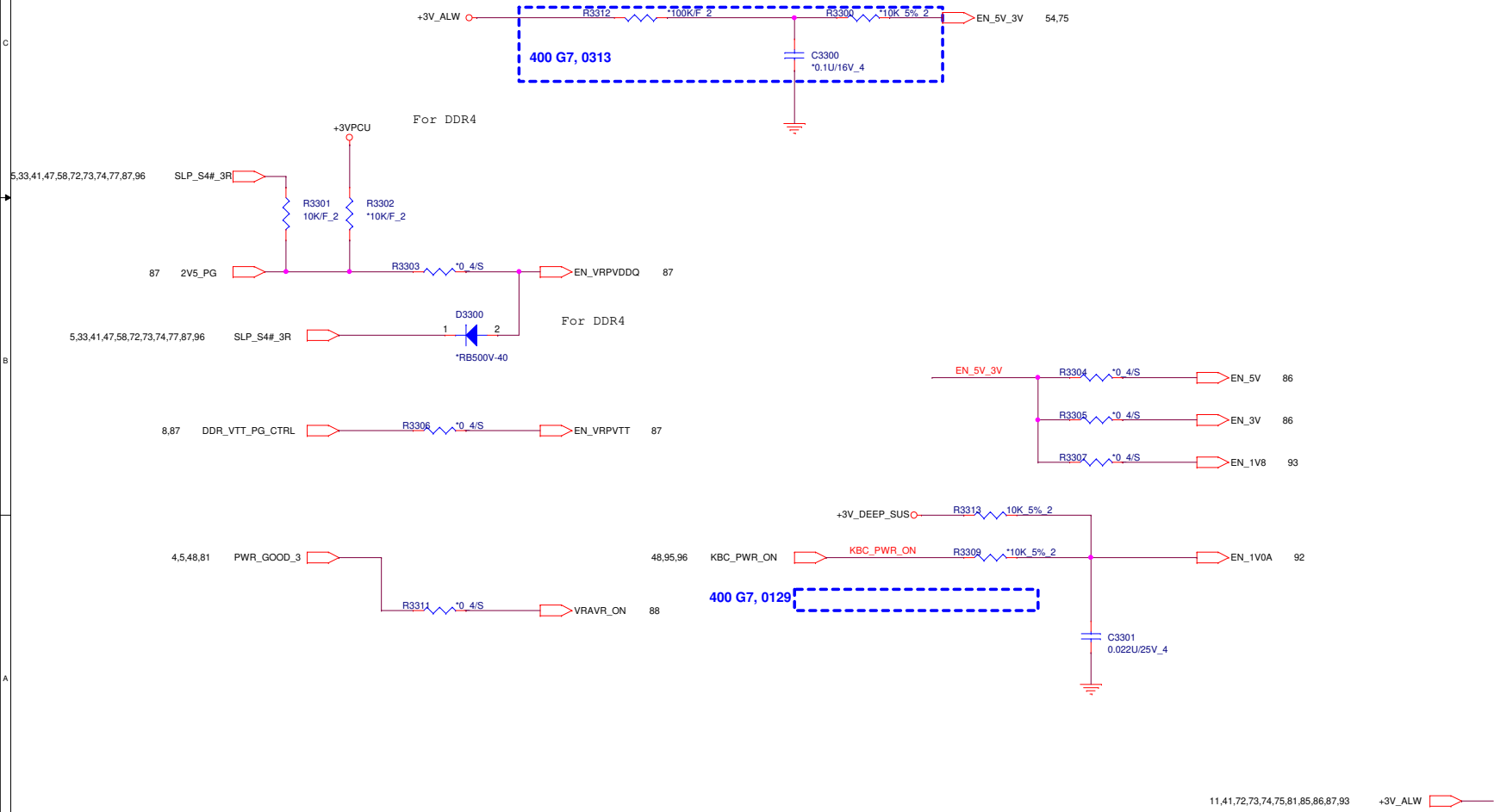







400 series 1001

POWER TO EE NET NAME CONNECTION





PROJECT : X8MA
Quanta Computer Inc.

Size Custom	Document Number 33 -- POWER ENABLE	Rev 3A
Date: Thursday, August 15, 2019		Sheet 33 of 106

20



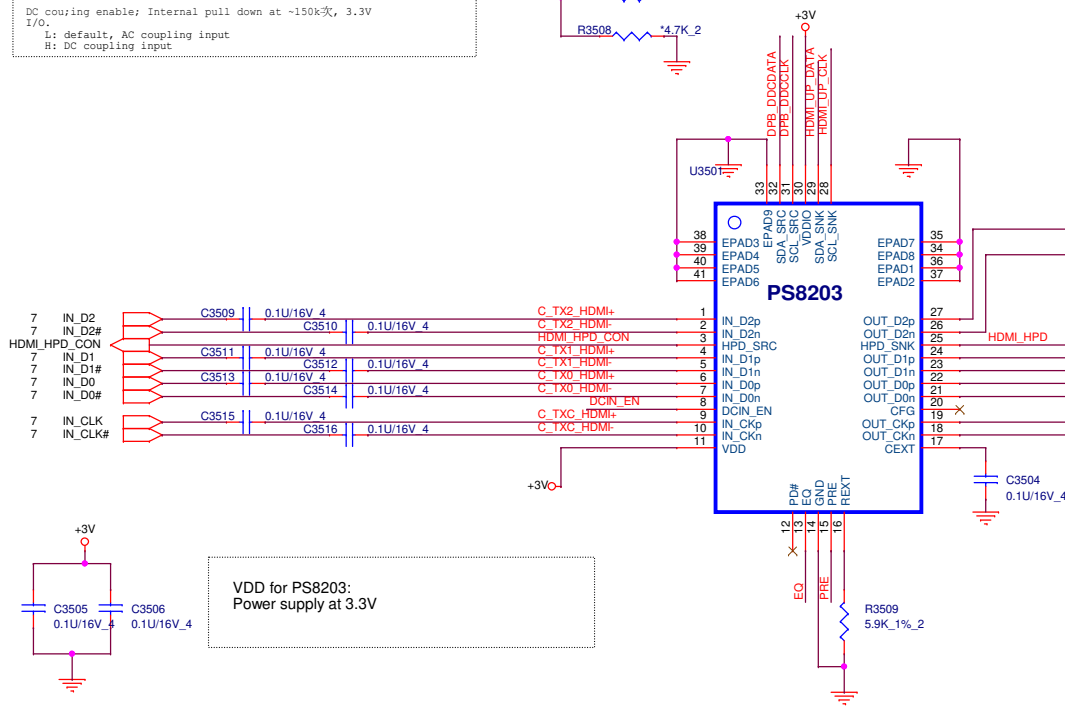
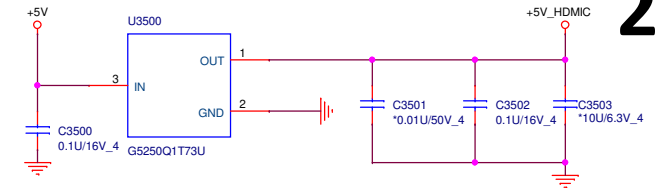
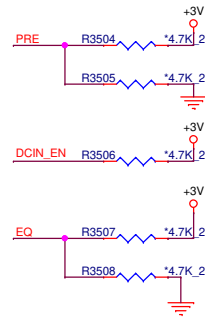
EMI Solution

TX2_HDMI+	R3500	*150_5%_4	TX2_HDMI-
TX1_HDMI+	R3501	*150_5%_4	TX1_HDMI-
TX0_HDMI+	R3502	*150_5%_4	TX0_HDMI-
TXC_HDMI+	R3503	*150_5%_4	TXC_HDMI-

Output pre-emphasis setting; Internal pull down at ~150k Ω , 3.3V I/O.
L: no pre-emphasis
H: 2.5dB pre-emphasis

Receiver equalization setting; Internal pull down at ~150k Ω , 3.3V I/O.
L: programmable EQ for channel loss up to 12.4dB @ 3Gbps
H: programmable EQ for channel loss up to 4.3dB @ 3Gbps
W: programmable EQ for channel loss up to 8.6dB @ 3Gbps

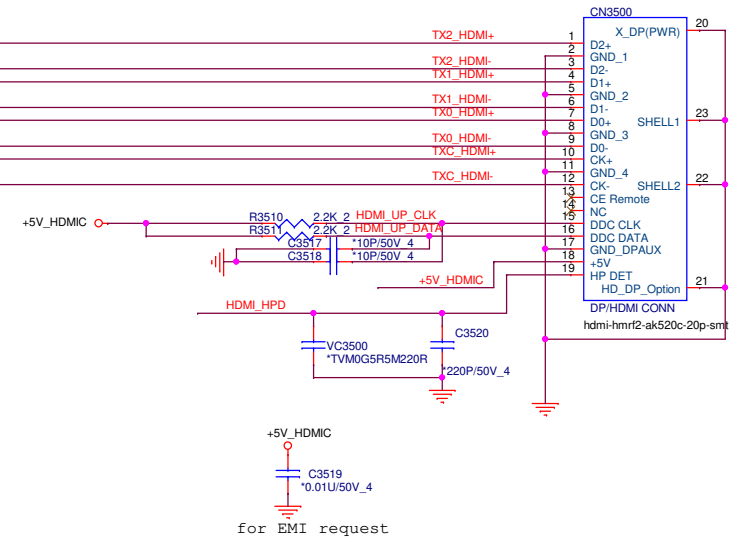
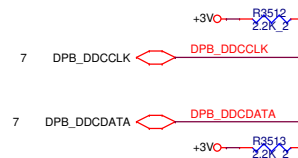
DC coupling enable; Internal pull down at ~150k Ω , 3.3V I/O.
L: default, AC coupling input
H: DC coupling input



VDD for PS8203:
Power supply at 3.3V

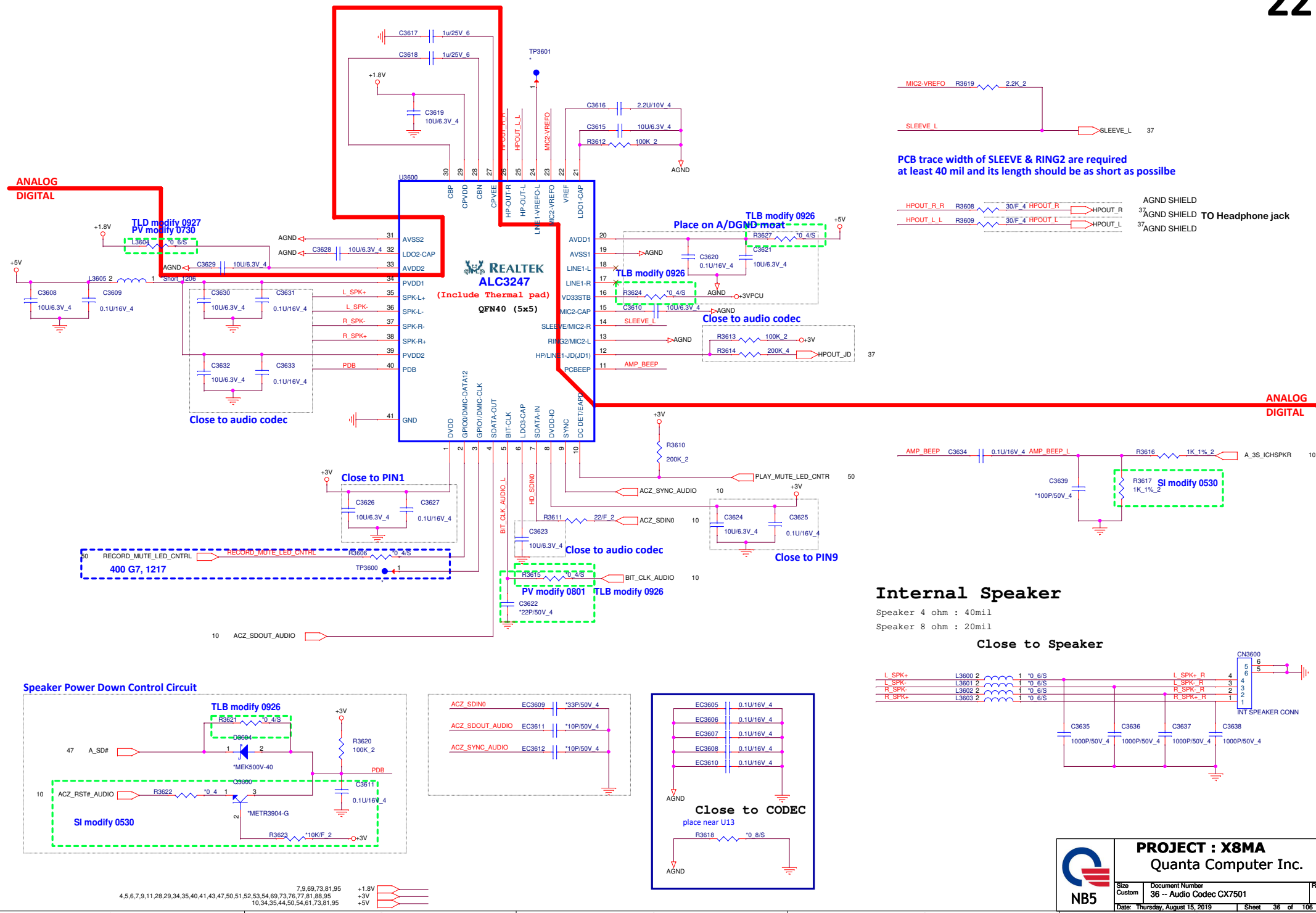
VDDIO:
Supply voltage for DDC passive gate and used to set HPD_SRC output level
Its range can be 1.2V~3.6V

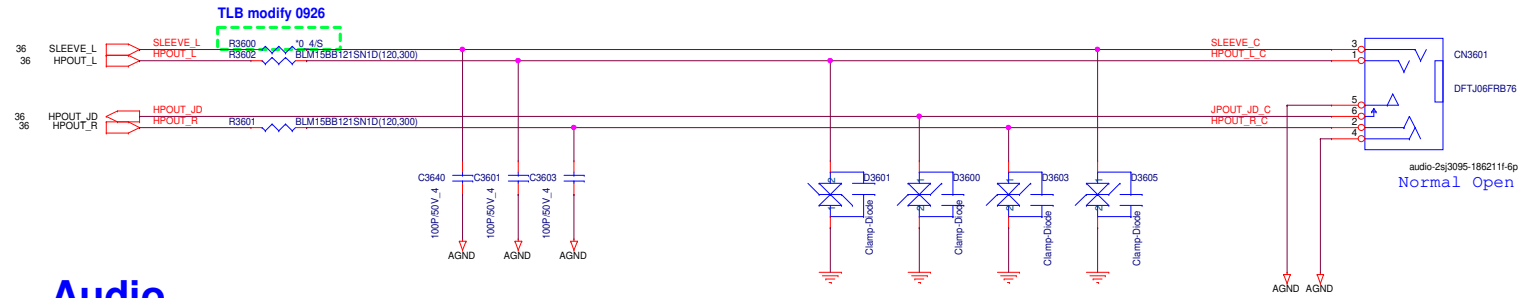
HDMI SMBus Isolation



PROJECT : X8MA
Quanta Computer Inc.

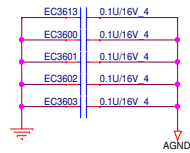
Size Custom	Document Number	Rev 3A
	35 -- HDMI CONNECTOR	
Date: Thursday, August 15, 2019	Sheet 35 of 106	






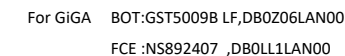
Audio

All Clamp-Diode need close to ADO Jack.

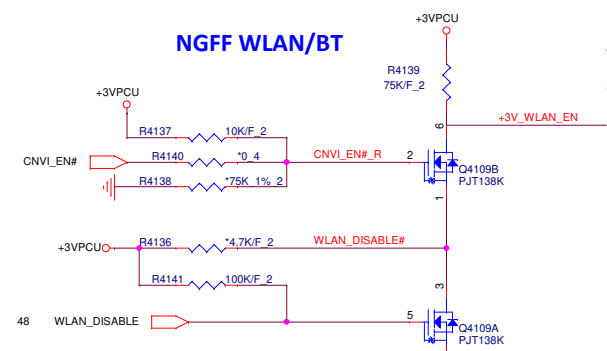


	PROJECT : X8MA	
	Quanta Computer Inc.	
	Size Custom Document Number 37 -- Audio JACK Date: Thursday, August 15, 2019	Rev 3A Sheet 37 of 106

24

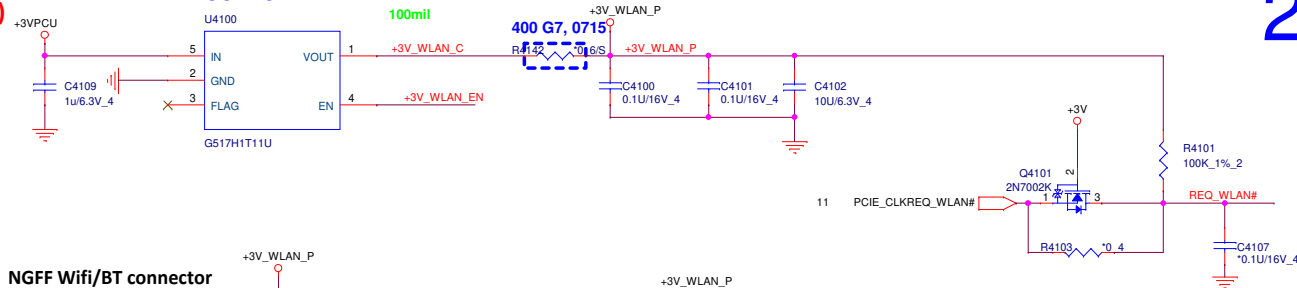


NGFF WLAN/BT

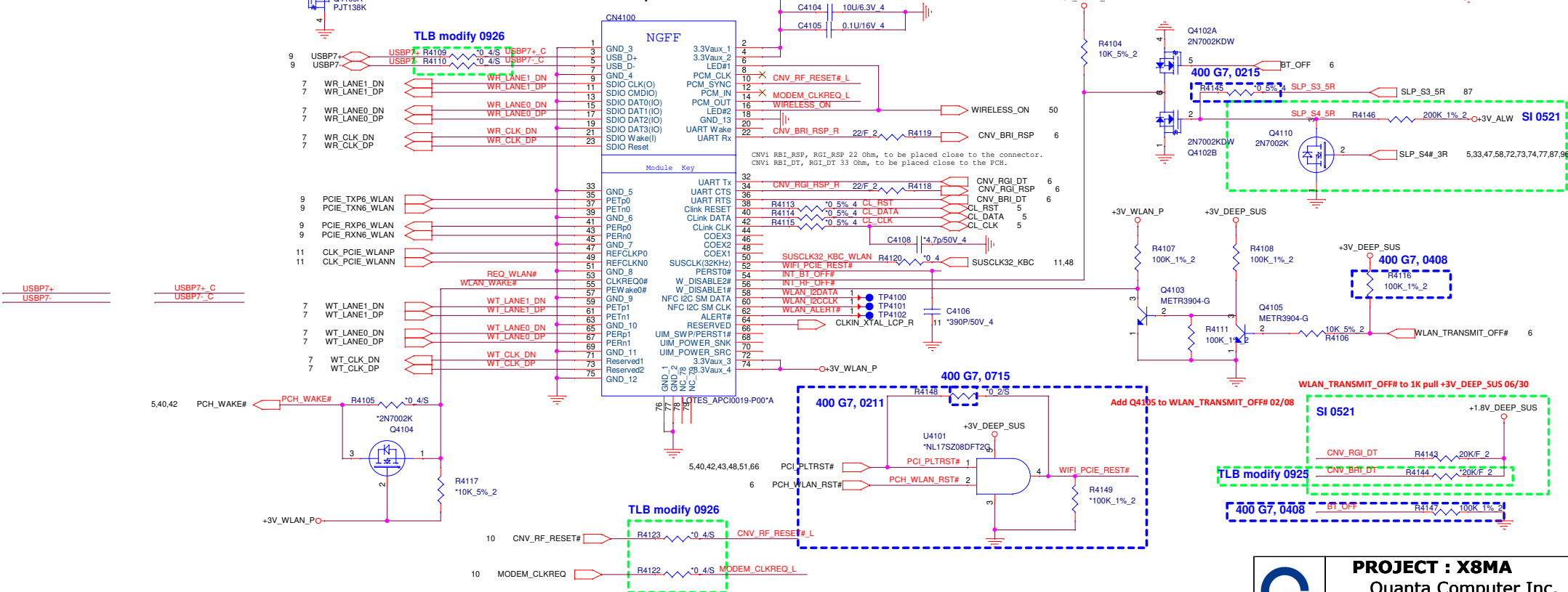


**Mini Card
WLAN/BT(Optional)
2.5A for WLAN**

OCP : 3.2A

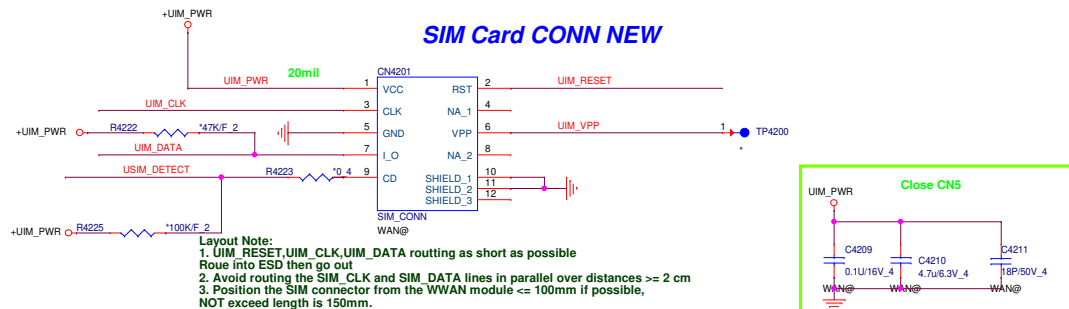
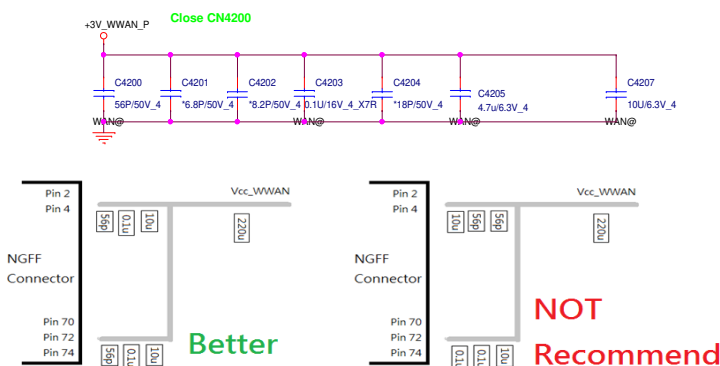
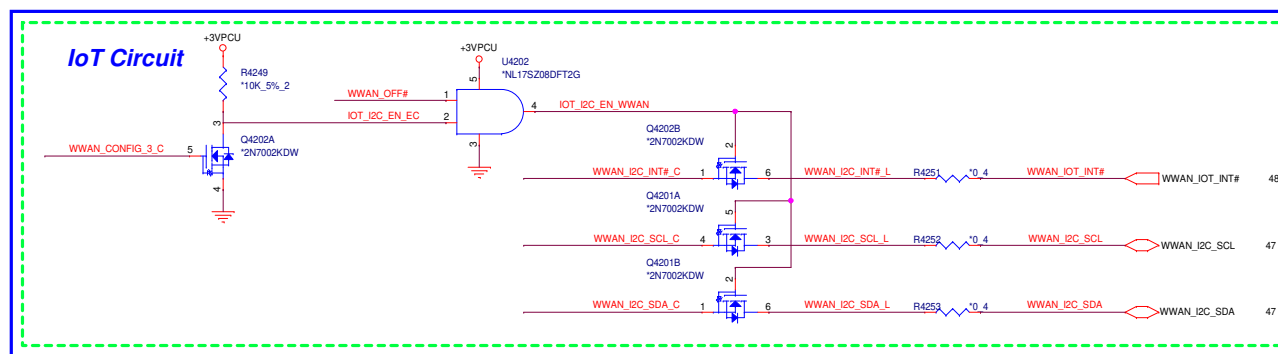
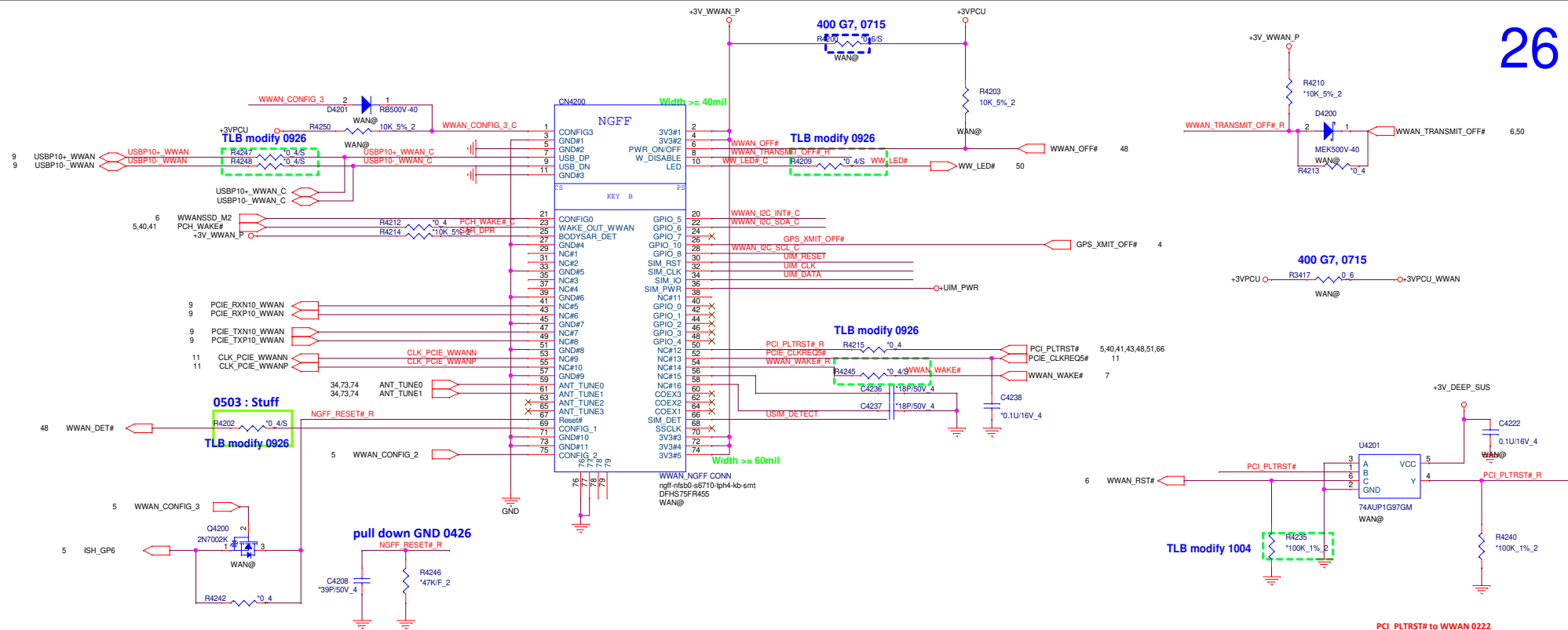


NGFF Wifi/BT connector



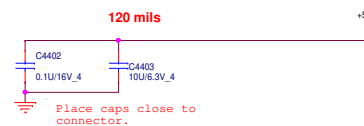
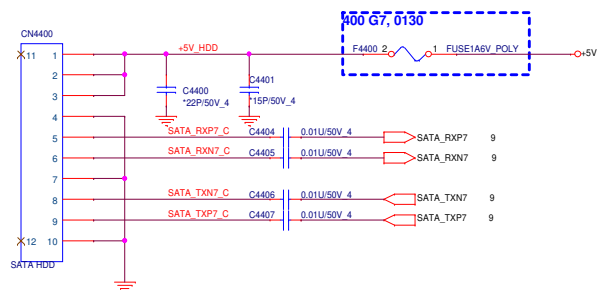
PROJECT : X8MA
Quanta Computer Inc.

Size Custom	Document Number 41 -- NGFF WLAN/BT	Rev 3A
Date: Thursday, August 15, 2019	Sheet 41 of 106	




+VCC	Power_On/Off (Pin6)	W_Disable (Pin8)	GPS_Disable (Pin26)
S0	High	High	High
S3 ON	High	Low	Low
S4 ON	Low	Low	Low
S5 ON	Low	Low	Low

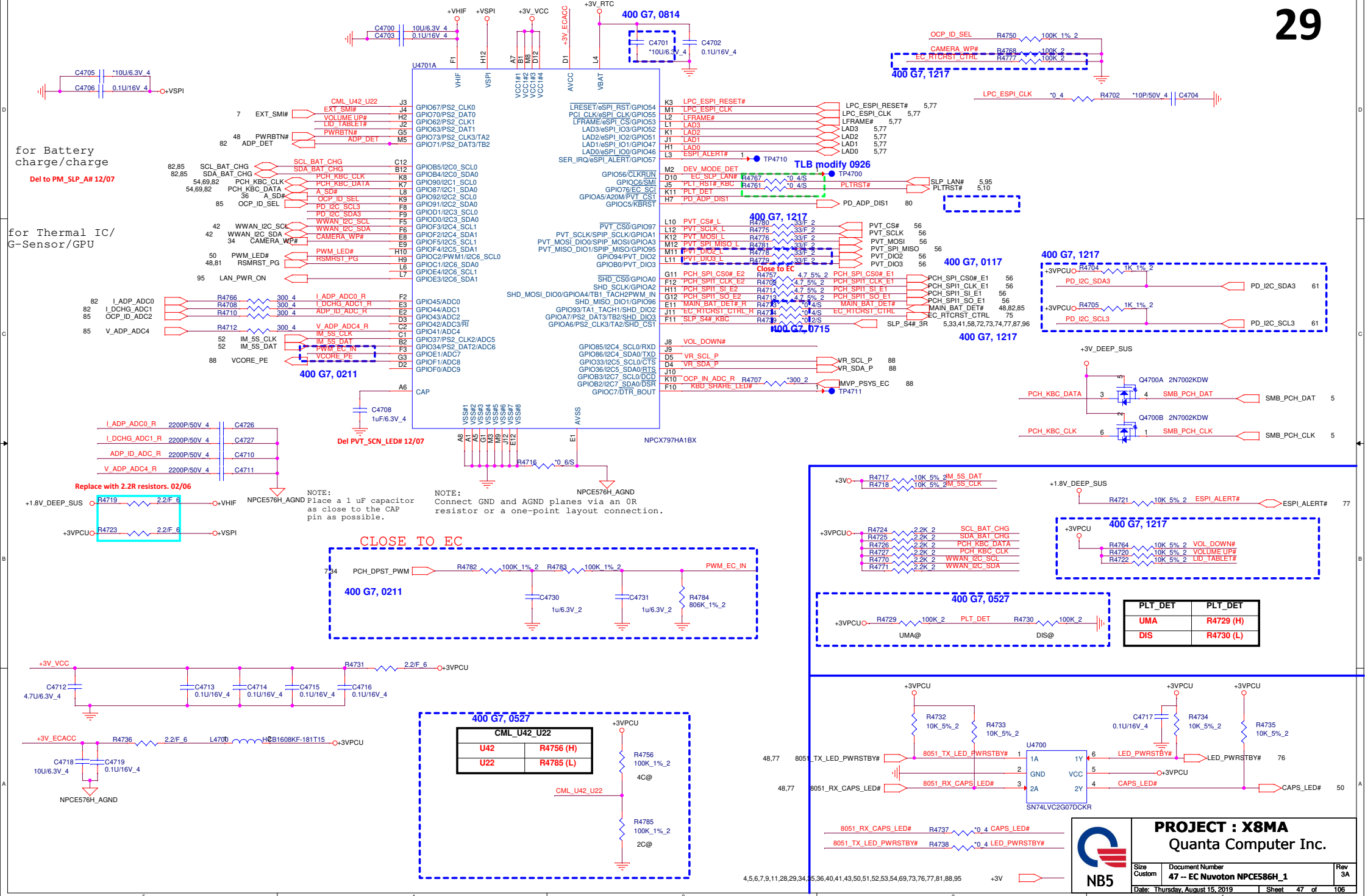
SATA-HDD

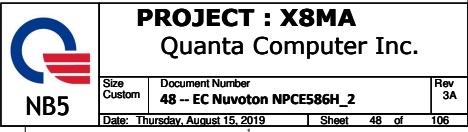


4,5,6,7,9,11,28,29,34,35,36,40,41,43,47,50,51,52,53,54,66,73,76,77,81,88,95
10,34,35,36,50,54,61,73,81,95

+3V
+5V

	PROJECT : X8MA Quanta Computer Inc.		
	Size C	Document Number 44 - HDD/EMI cap	Rev 3A
Date: Thursday, August 15, 2018		Sheet 44 of 106	





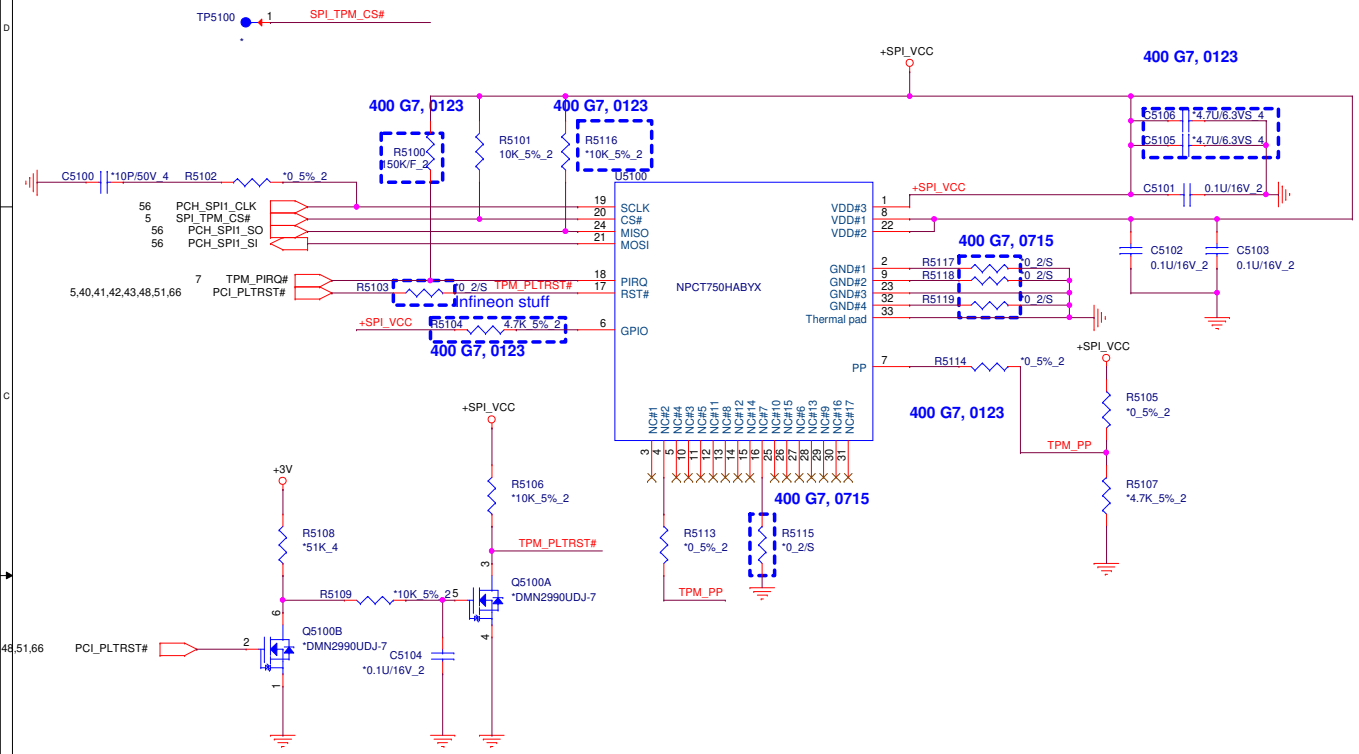



TPM (1.2 or 2.0)

32

AL000750004 AL009670042

	Nuvoton	Infineon
C5106	V	
C5105	V	
R5116	V	
R5113	V	
R5115	V	
R5117		V
R5118		V
R5119		V
R5114		V
R5104		V
R5100	10K	150K



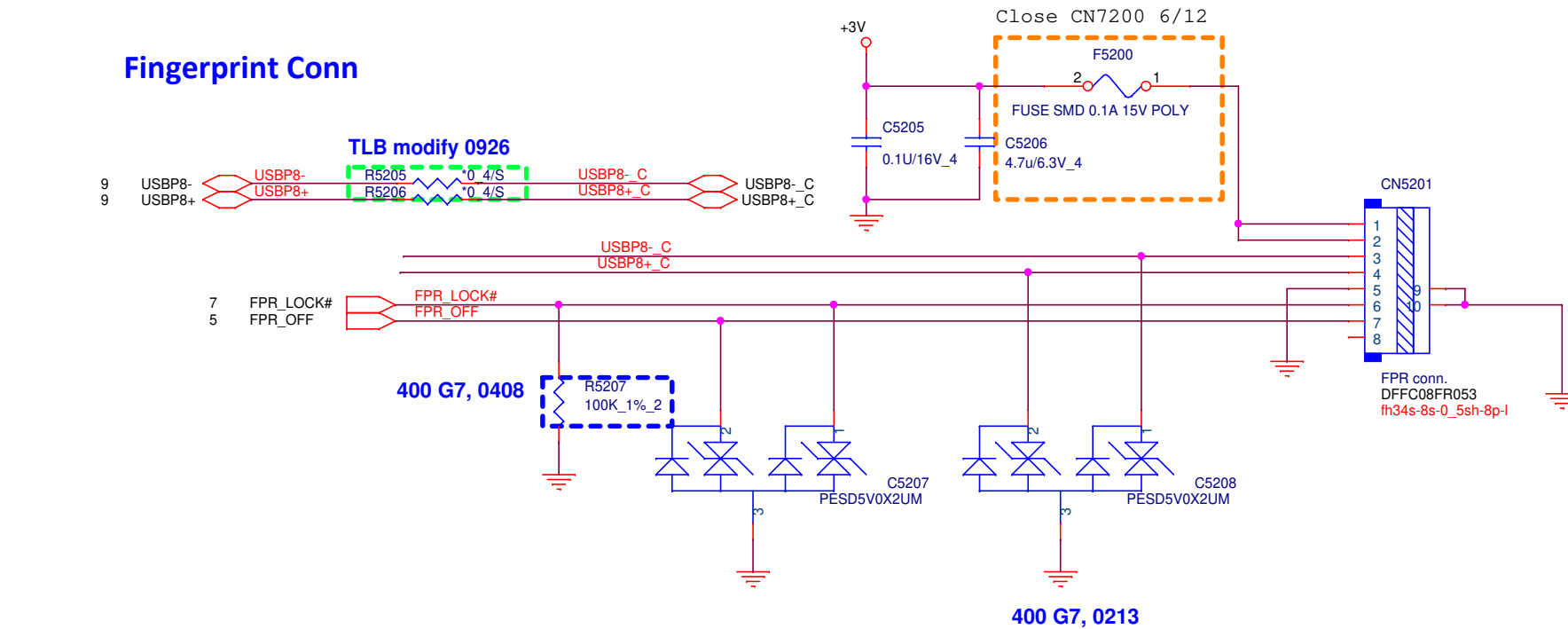


PROJECT : X8MA

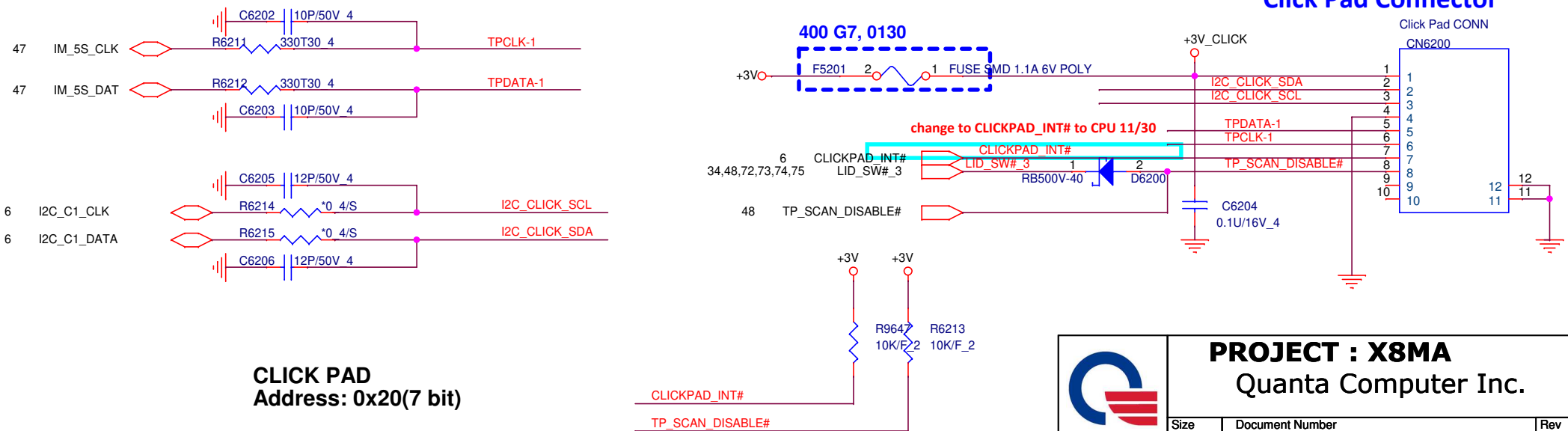
Quanta Computer Inc.

Size Custom	Document Number 51 -- TPM SLB9670_QFN	Rev 3A
Date: Thursday, August 15, 2019	Sheet 51 of 106	

Fingerprint Conn



Click Pad Connector



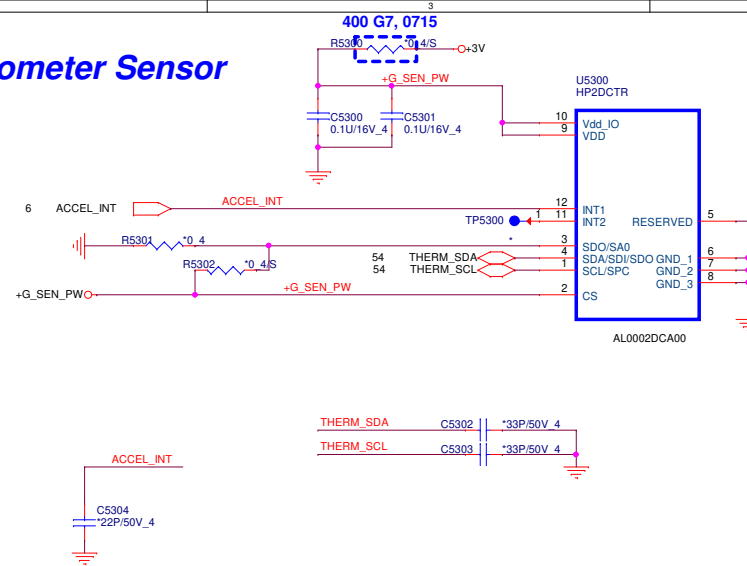
CLICK PAD
Address: 0x20(7 bit)




PROJECT : X8MA
Quanta Computer Inc.

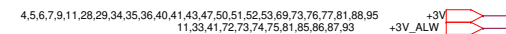
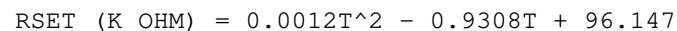
Size Custom	Document Number 52 -- FPR / Click PAD	Rev 3A
Date: Thursday, August 15, 2019	Sheet 52 of 106	

Accelerometer Sensor



4,5,6,7,9,11,28,29,34,35,36,40,41,43,47,50,51,52,54,69,73,76,77,81,88,95 +3V
5,7,12,33,34,36,41,42,47,48,50,54,56,58,61,73,74,75,77,80,81,82,85,86,87,88,92,93,95,105 +3VPCU

	PROJECT : X8MA Quanta Computer Inc.		
	Size Custom	Document Number 53 -- TS and Accelerometer	Rev 3A
	Date: Thursday, August 15, 2019		Sheet 53 of 106

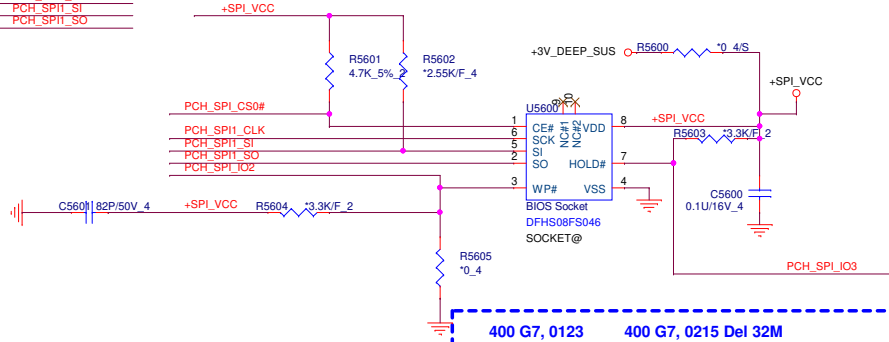


SPI ROM

Vender	Size	P/N
MXIC	128MB	AKE3DZKNZ00
Winbond	128MB	AKE3DF-KN00 Pilot run stage
Socket		DFHS08FS046
MXIC	128MB	AKE3DZN0Z08 MV stage
Winbond	128MB	AKE3DF-KN01

PCH SPI ROM(CLG) Place TP at TOP side

TP5600	1	PCH_SPI_CS0#
TP5601	1	PCH_SPI_CLK
TP5602	1	PCH_SPI_SI
TP5603	1	PCH_SPI_SO



PCH 6*5mm WSON 16M SPI ROM Socket

400 G7, 0123 400 G7, 0215 Del 32M

PCH_SPI_SI
PCH_SPI_SO
PCH_SPI_CS0#
PCH_SPI_CLK

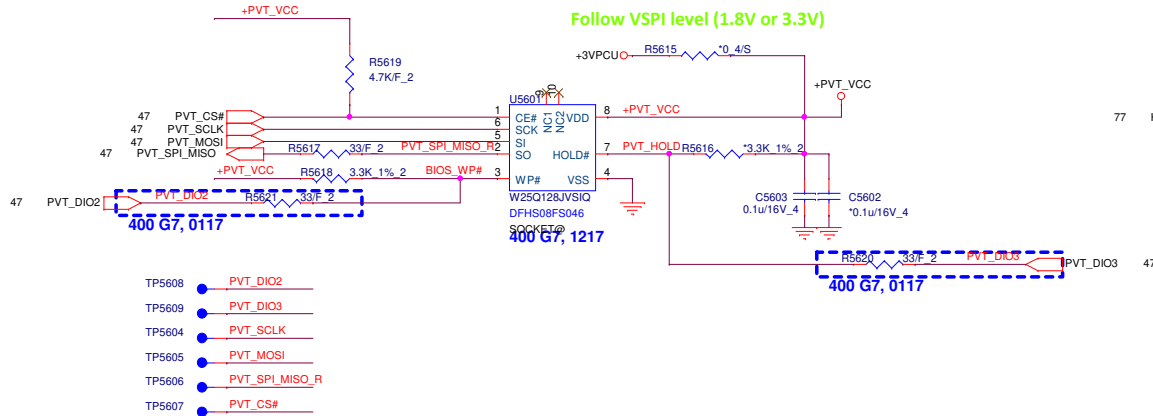
+SPL_VCC
PCH_SPI_IO2
PCH_SPI_IO3

EC SPI ROM

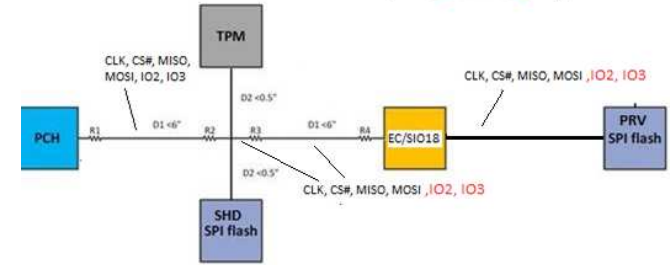
Vender	Size	P/N
GD	128MB	AKE2DF00Q00 Pilot run stage
GD	128MB	AKE3DZN0Q02 MV stage

EC SPI ROM Socket WSON 16M 6x5

Follow VSPI level (1.8V or 3.3V)



TP5608	PVT_DIO2
TP5609	PVT_DIO3
TP5604	PVT_SCLK
TP5605	PVT_MOSI
TP5606	PVT_SPI_MISO_R
TP5607	PVT_CS#

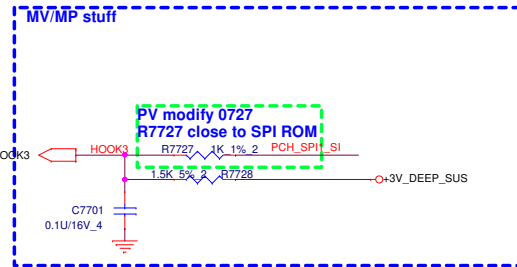


nuvoton

Nuvoton Confidential - Provided under NDA

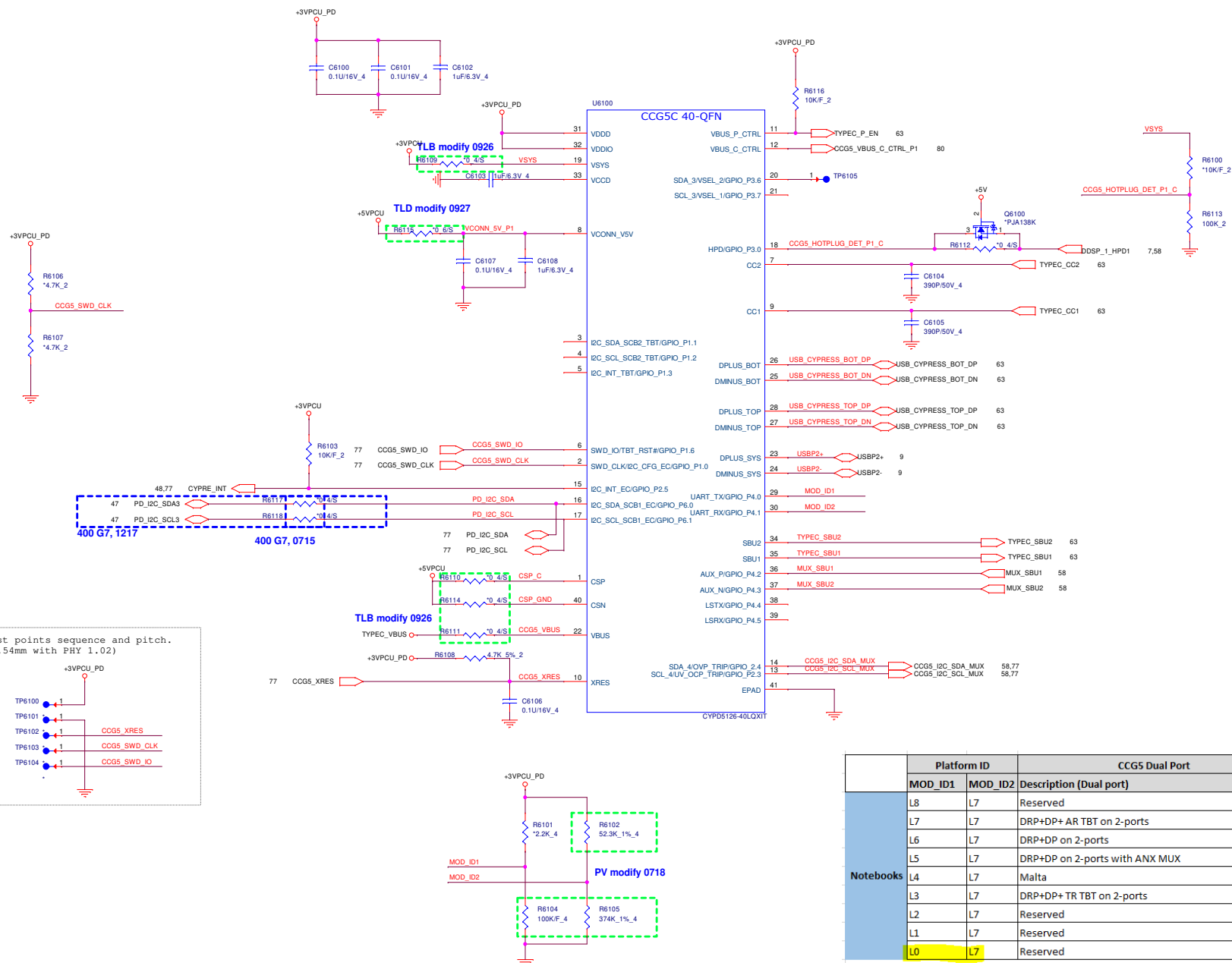
Based on EC18 testing: PCH to TPM/SPI flash = Quad I/O, SIO18 to SPI Flash = Dual I/O, Quad I/O, R1 = 4.7 ohm for CLK, CS#, MISO, MOSI; R1 = 0 ohm for IO2, IO3 R2 = 22 ohm for CLK, CS#, MISO, MOSI; R2 = 15 ohm for IO2, IO3 R3 = 22 ohm for CLK, CS#, MISO, MOSI; R3 = for IO2, IO3 22 ohm! R4 = 4.7 ohm for CLK, CS#, MISO, MOSI; R4 = for IO2, IO3 4.7 ohm Use same values to start on IO2 and IO3

Note: The value of the resistors should be tuned according to the signal integrity simulations or actual PCB measurements.



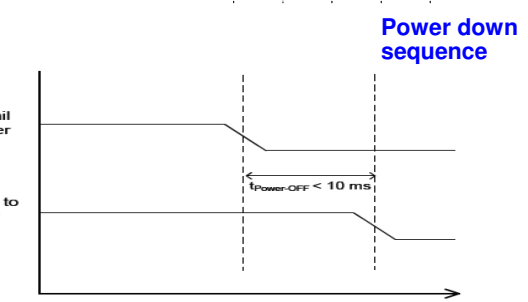
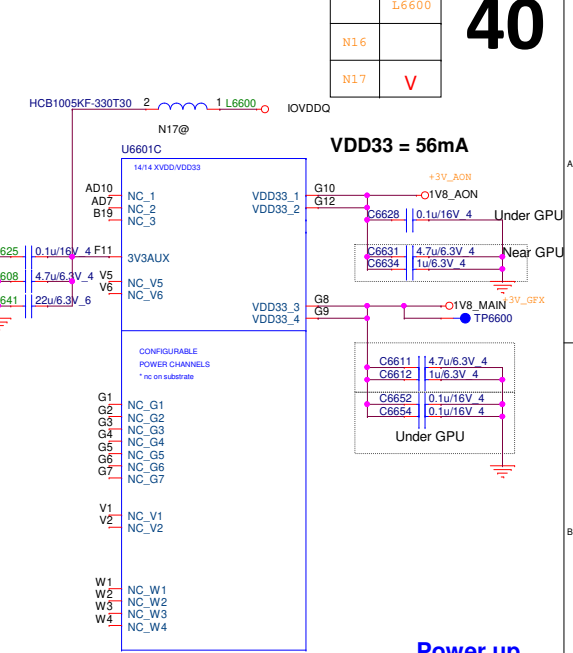
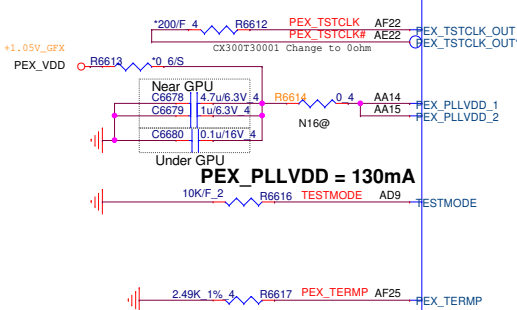
PROJECT : X8MA
Quanta Computer Inc.

Size Custom	Document Number 56 - Flash(KBC+PCH)	Rev 3A
Date: Thursday, August 15, 2019	Sheet 56 of 106	




	Platform ID		CCG5 Dual Port	CCG5/CCG5C Single Port	L0 = 0V
	MOD_ID1	MOD_ID2	Description (Dual port)	Description (Single Port)	L1 = VDD0/8
Notebooks	L8	L7	Reserved	DRP+USB on 1-port with No MUX	L2 = 2* VDD0/8
	L7	L7	DRP+DP+ AR TBT on 2-ports	DRP+DP on 1-port with ANX MUX	L3 = 3* VDD0/8
	L6	L7	DRP+DP on 2-ports	DRP+DP+ TR TBT on 1-port	L4 = 4* VDD0/8
	L5	L7	DRP+DP on 2-ports with ANX MUX	DRP+DP+ AR TBT on 1-port (700, 800 Series)	L5 = 5* VDD0/8
	L4	L7	Malta	DRP+DP on 1-port with Parade MUX	L6 = 6* VDD0/8
	L3	L7	DRP+DP+ TR TBT on 2-ports	DRP+DP on 1-port (600/700 Series) - AMD SKU1	L7 = 7* VDD0/8
	L2	L7	Reserved	DRP+DP on 1-port (600/700 Series) - AMD SKU2	L8 = VDD0
	L1	L7	Reserved	DRP+DP on 1-port (600/700 Series) - AMD SKU3	
	L0	L7	Reserved	DRP+DP on 1-port with Parade MUX - 2019 S400 G6	

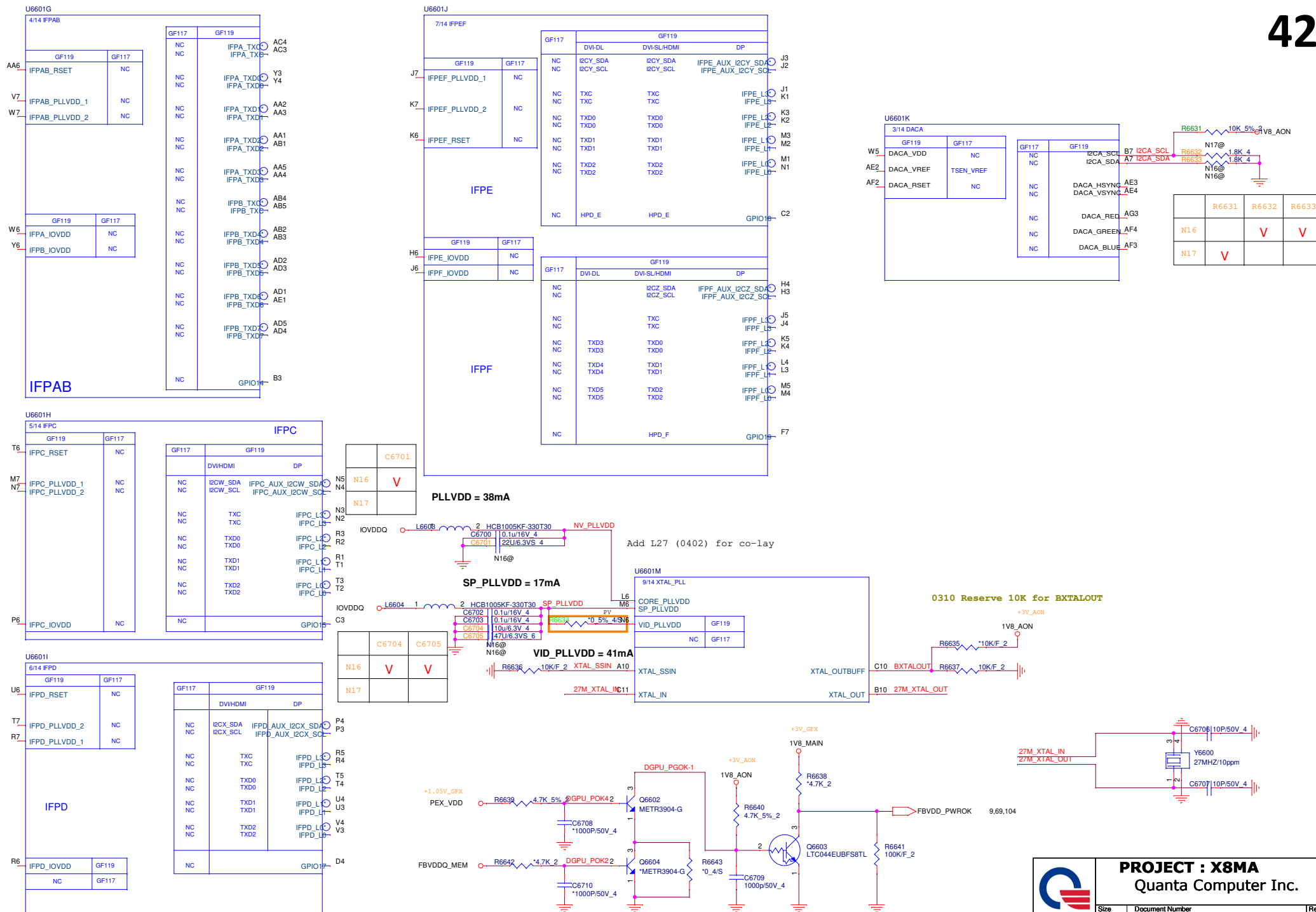




First Rail to Power Down

 NB5	PROJECT : X8MA Quanta Computer Inc.		
	Size Custom	Document Number N17S-G1-A1(PCIE I/F)/NVDD	Rev
	Date: <u>Thursday, August 15, 2019</u>		Sheet <u>66</u> of <u>106</u>





Channel A <0-31>
MF=0 Non-mirrored**CHANNEL A: 2G GDDR5****Channel A <32-63>**
MF=0 Non-mirrored

QD24~31

QD16~23

QD8~15

QD0~7

QD56~63

QD48~55

QD40~47

QD32~39

Boundary Scan
Place Top side

FBA_CMD13
FBA_CMD0
FBA_EDC0
SEN_A0
MF_A0

FBA_CMD29
FBA_CMD16
FBA_EDC4
SEN_A2
MF_A2

For layout
Del TP symbol and add TP on VIA**PROJECT : X8MA**
Quanta Computer Inc.

Size	Document Number	Rev
Custom	23 - VRAM GDDR5 - RANK1	1A
Date: Thursday, August 15, 2019	Sheet 70 of 106	

Table 9.5 GDDR5 DEBUG Command Lines

Command Ball on GPU	DRAM Signal Definition
FBA_CMD32 (do not connect to DRAM)	(not used)
FBA_CMD33 (do not connect to DRAM)	(not used)
FBA_CMD34 (do not connect to DRAM)	DEBUG0
FBA_CMD35 (do not connect to DRAM)	DEBUG1

Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

Table 9.4 GDDR5 Command Mapping (GB4C-128 & GB2C-64 packages)

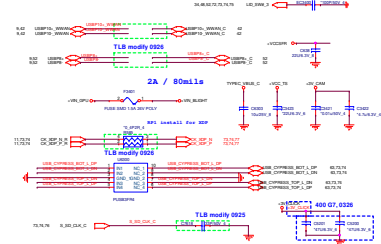
Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CS*
FBA_CMD1	FBA_CMD17	A3_BA3
FBA_CMD2	FBA_CMD18	A2_BA0
FBA_CMD3	FBA_CMD19	A4_BA2
FBA_CMD4	FBA_CMD20	A5_BA1
FBA_CMD5	FBA_CMD21	WE*
FBA_CMD6	FBA_CMD22	A7_A8
FBA_CMD7	FBA_CMD23	A6_A11
FBA_CMD8	FBA_CMD24	AB1*
FBA_CMD9	FBA_CMD25	A12_RFU
FBA_CMD10	FBA_CMD26	A0_A10
FBA_CMD11	FBA_CMD27	A1_A9
FBA_CMD12	FBA_CMD28	RAS*
FBA_CMD13	FBA_CMD29	RST*
FBA_CMD14	FBA_CMD30	CKE*
FBA_CMD15	FBA_CMD31	CAS*

Table 4. N17S-LG/-G1 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35V	Samsung	K4G80325FB-HC28	B-die	0x0	7 Gbps	N/A	Full	Production candidate
			Micron	MT51J256M32HF-70:A	A-die	0x1	7 Gbps	N/A	Full	Production candidate
			Hynix	H5GC8H24MJR-R0C	M-die	0x2	7 Gbps	N/A	Full	Post production candidate
4 Gb	128Mx32	1.35V	Hynix	H5GC4H24AJR-R0C	A-die	0x6	7 Gbps	N/A	Full	Production candidate
			Samsung	K4G41325FE-HC28	E-die	0x7	7 Gbps	N/A	Full	Production candidate
			Micron	EDW4032BABG-70-F	A-die	0x8	7 Gbps	N/A	Full	Post production candidate

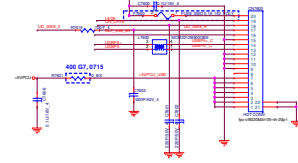
14"15" DIS only

EMI CAP



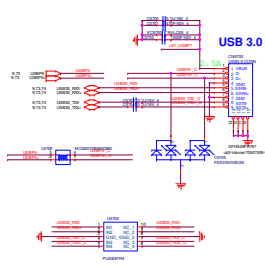
USB LID Daughter Board Connector

14"15" Used



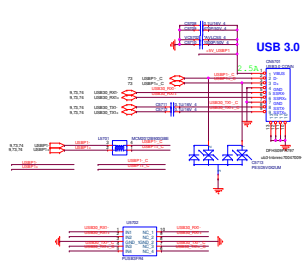
USB 2.0/3.0 Combo

14"15" Used

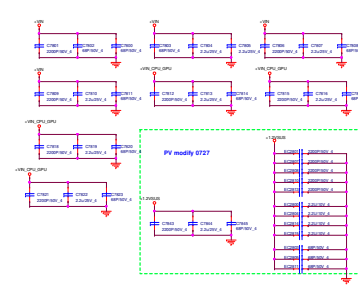


USB 2.0/3.0 Combo

USB 3.0

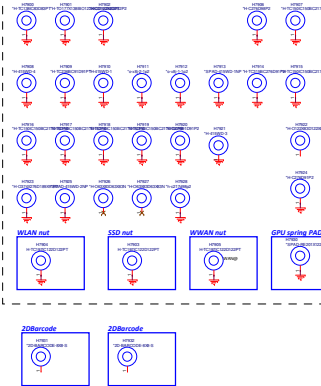


RF Cap

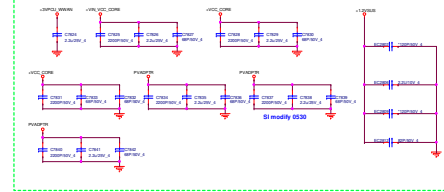


Shielding CAP

14"15 Hole

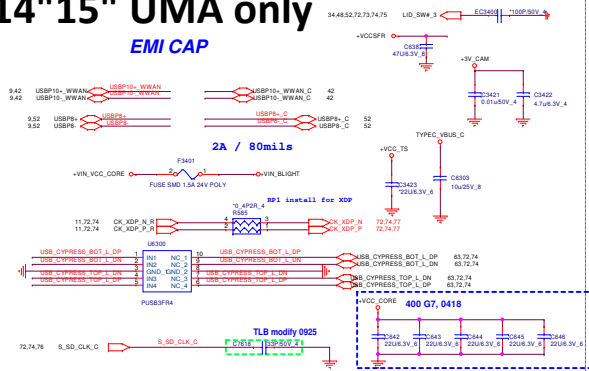


WWAN ONLY

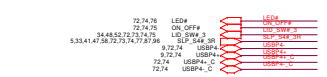


14"15" UMA only

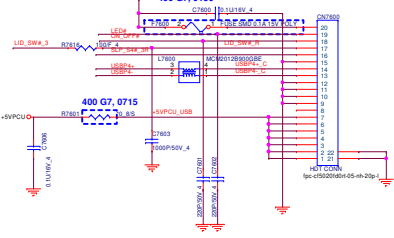
EMI CAP



USB LID Daughter Board Connector

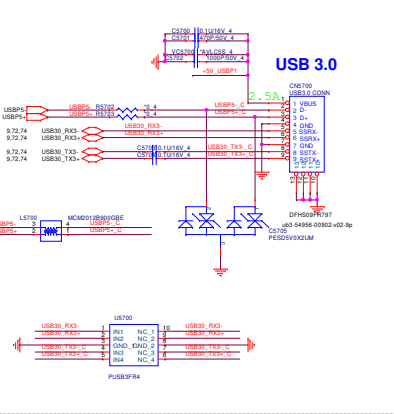


14"15" Used

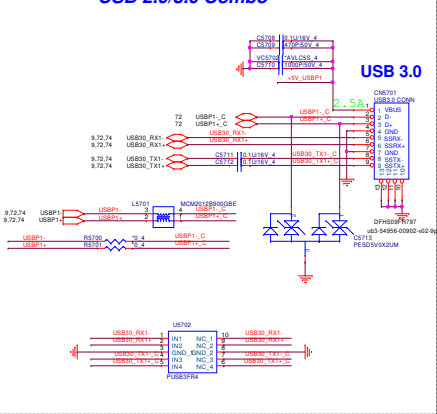


USB 2.0/3.0 Combo

14"15" Used

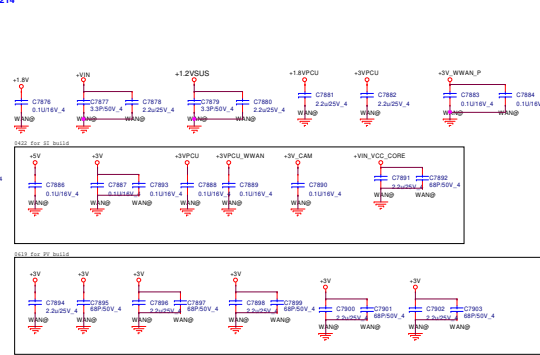


USB 2.0/3.0 Combo



400 G7, 0214

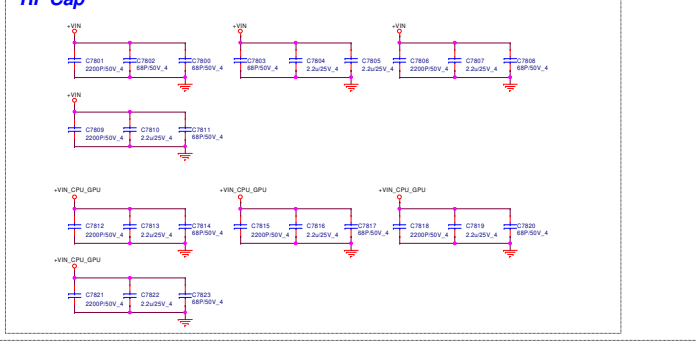
RF Cap



400 G7, 0129

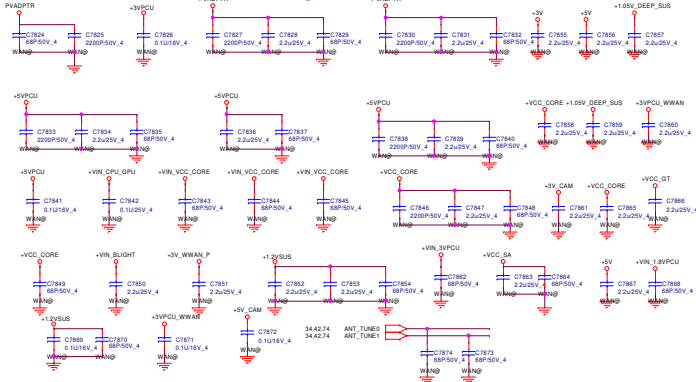


RF Cap

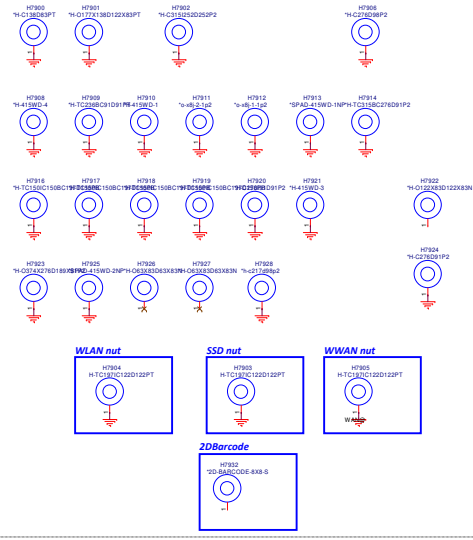


14 UMA RF Cap

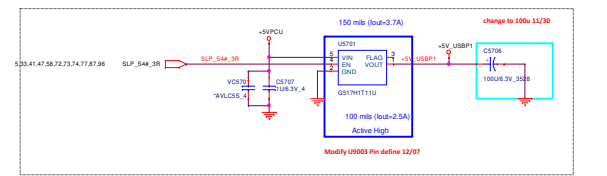
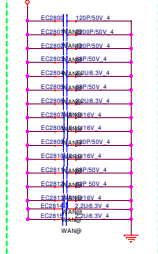
WWAN ONLY

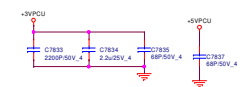
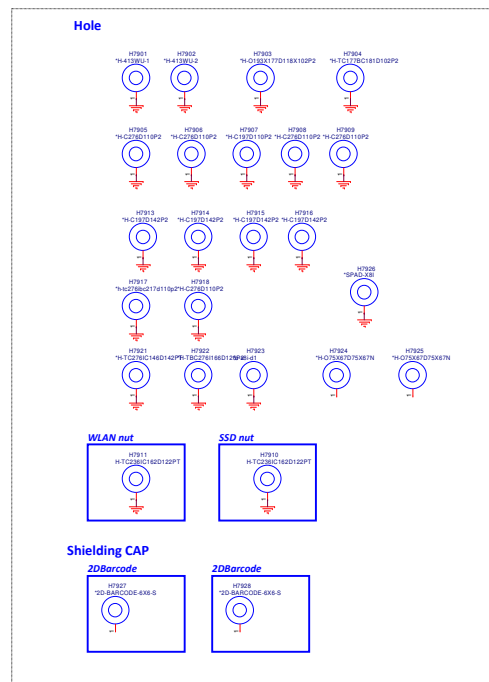
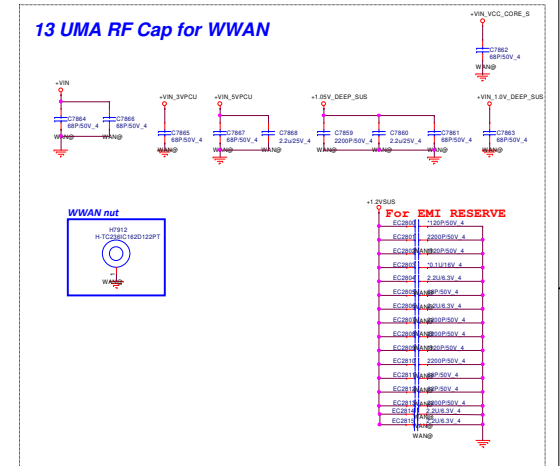
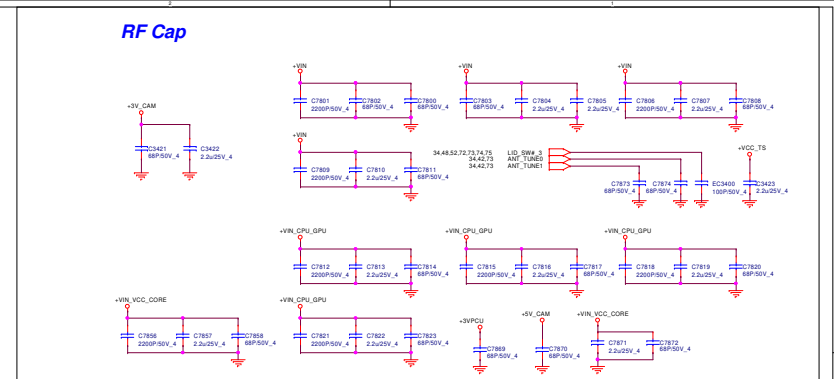
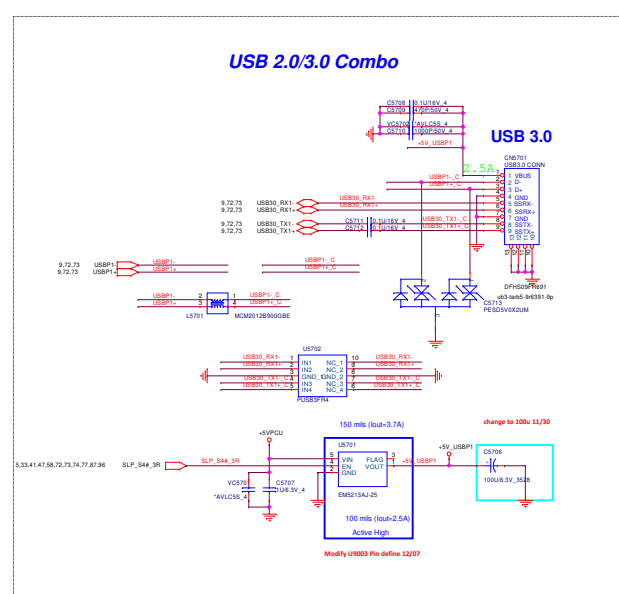
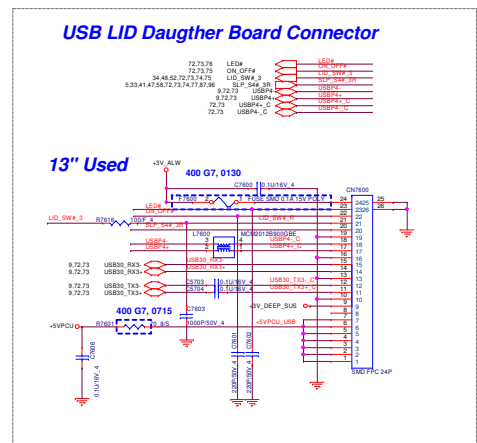


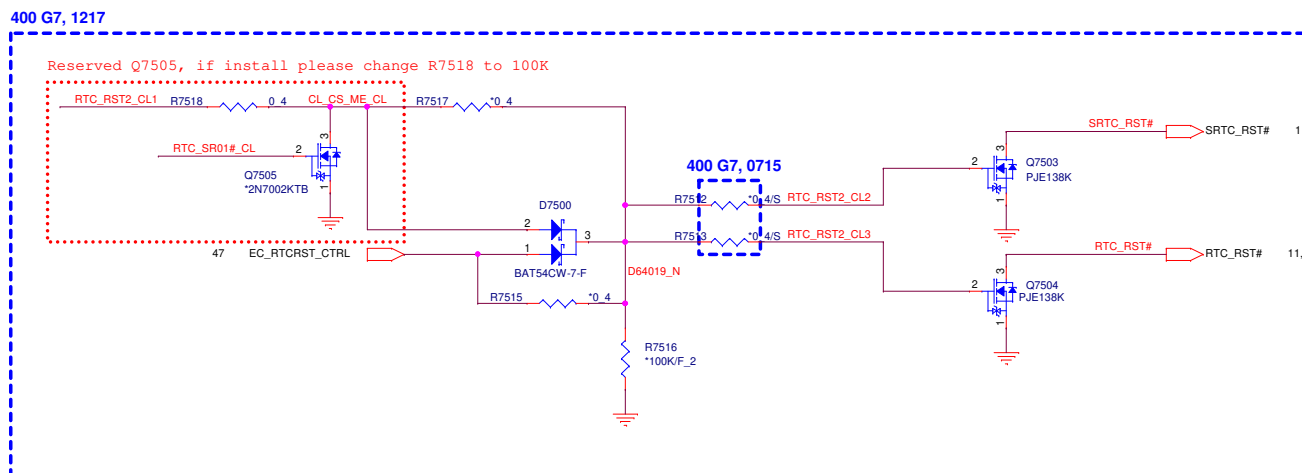
14"15 Hole



WWAN ONLY

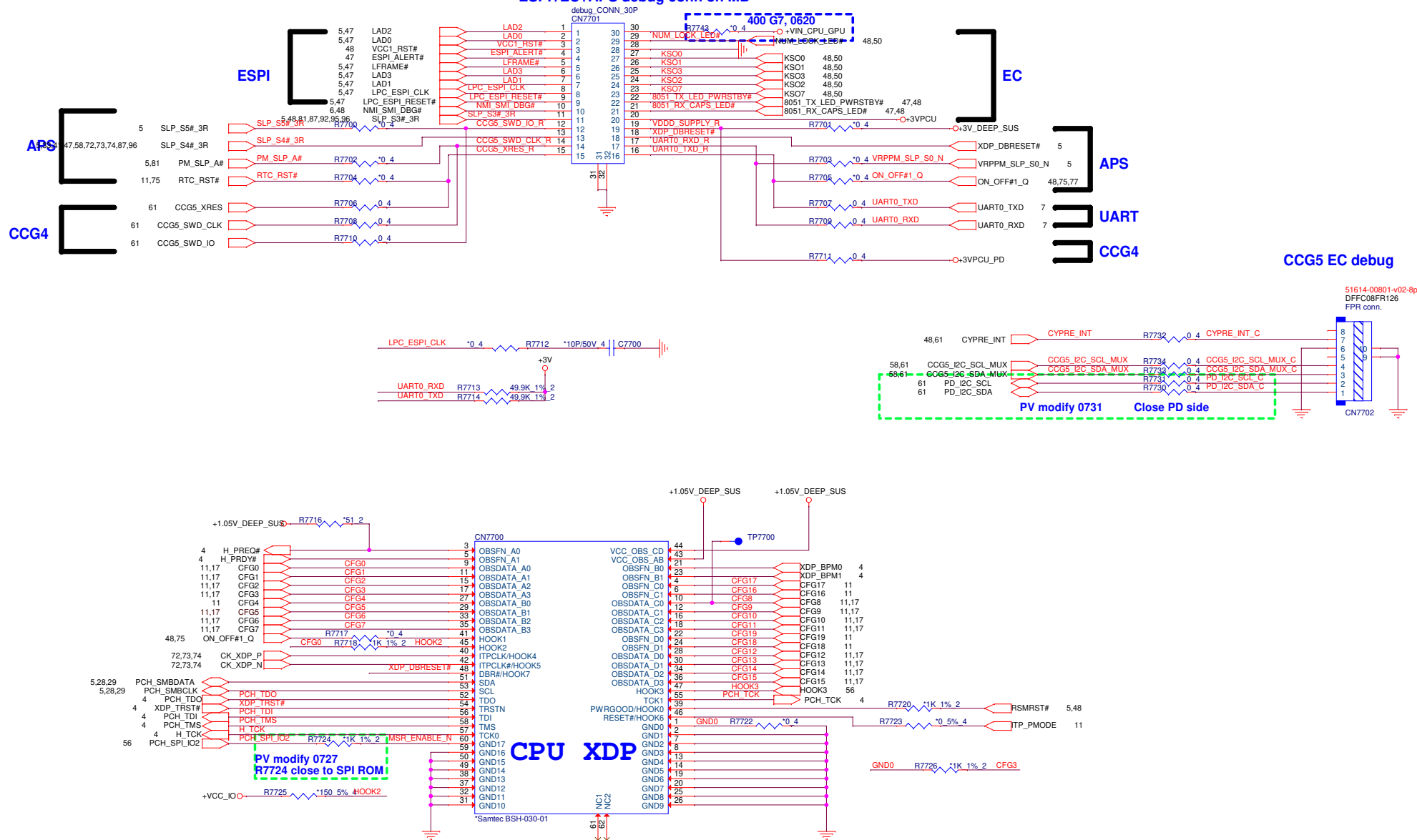







[illegible][illegible]

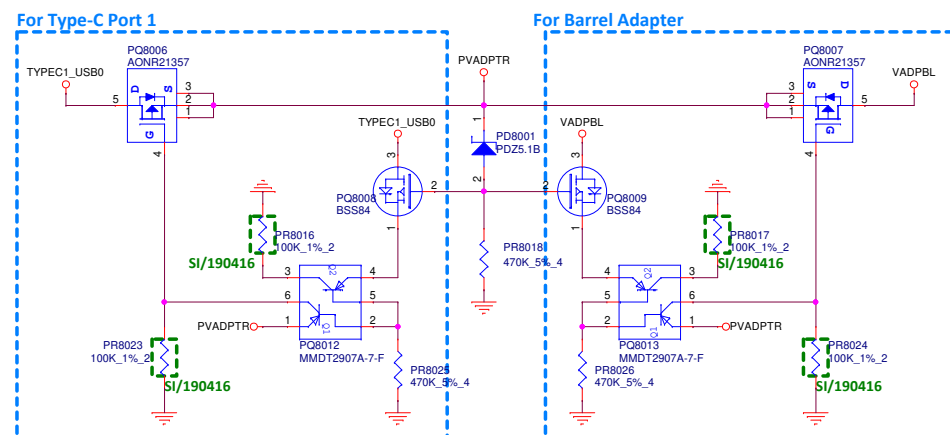
ESPI+EC+APS debug conn on MB

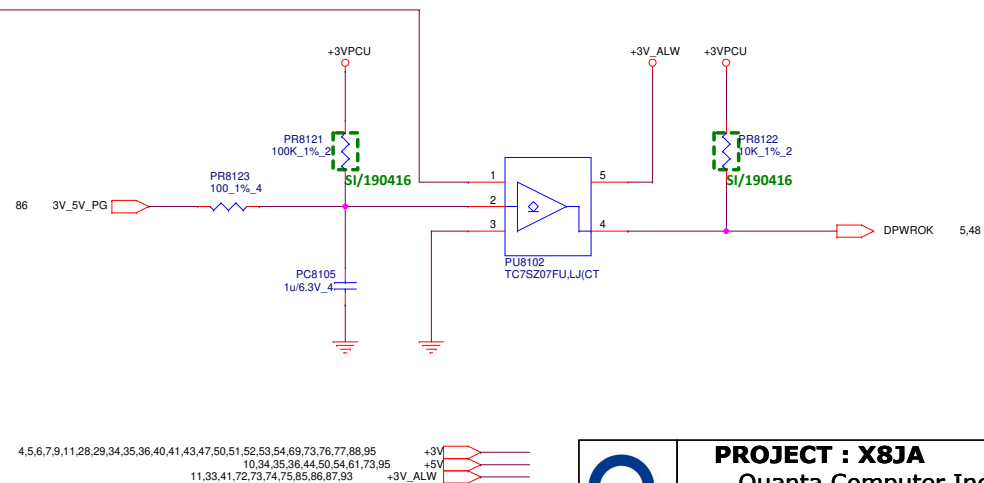
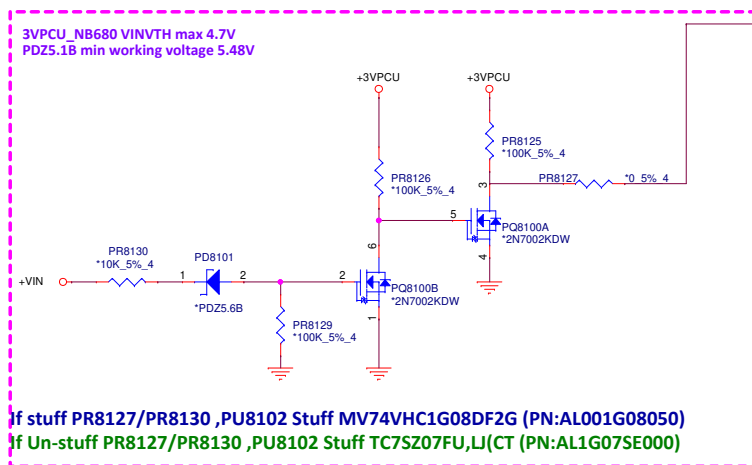
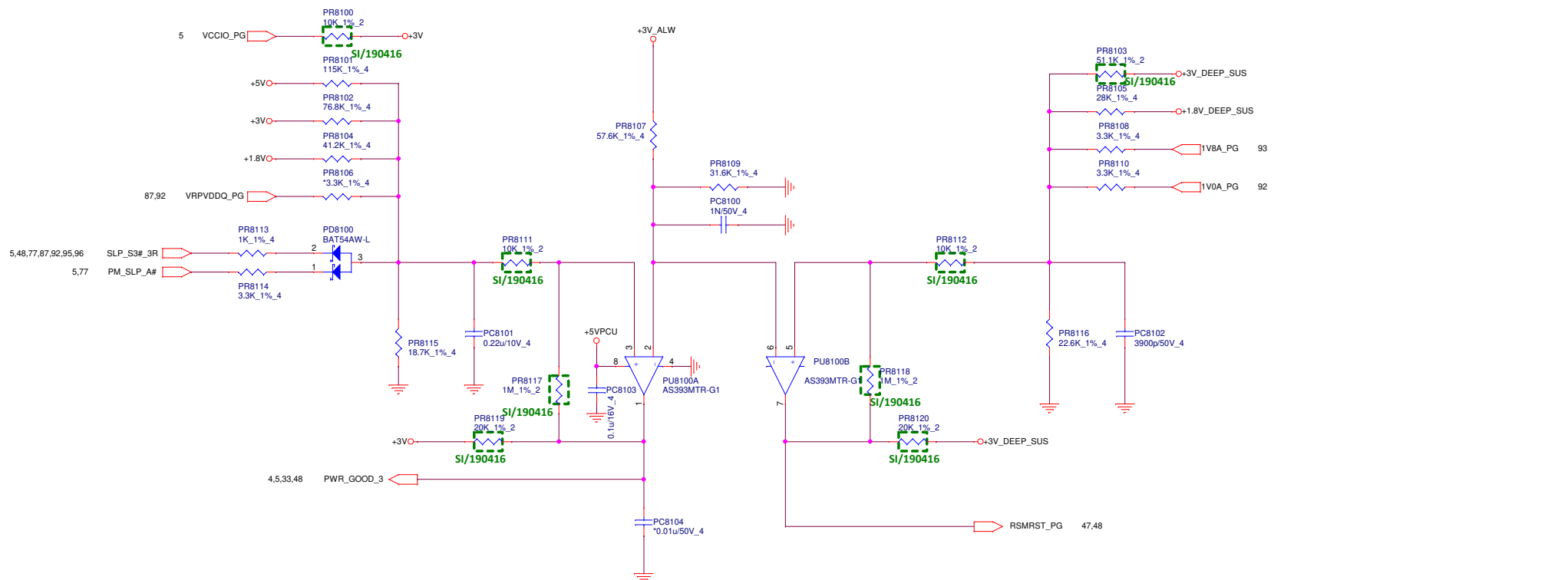





PROJECT : X8MA
Quanta Computer Inc.

Size Custom	Document Number 25 -- LVDS converter RTD2136	Rev 3A
Date: Thursday, August 15, 2019		Sheet 79 of 106

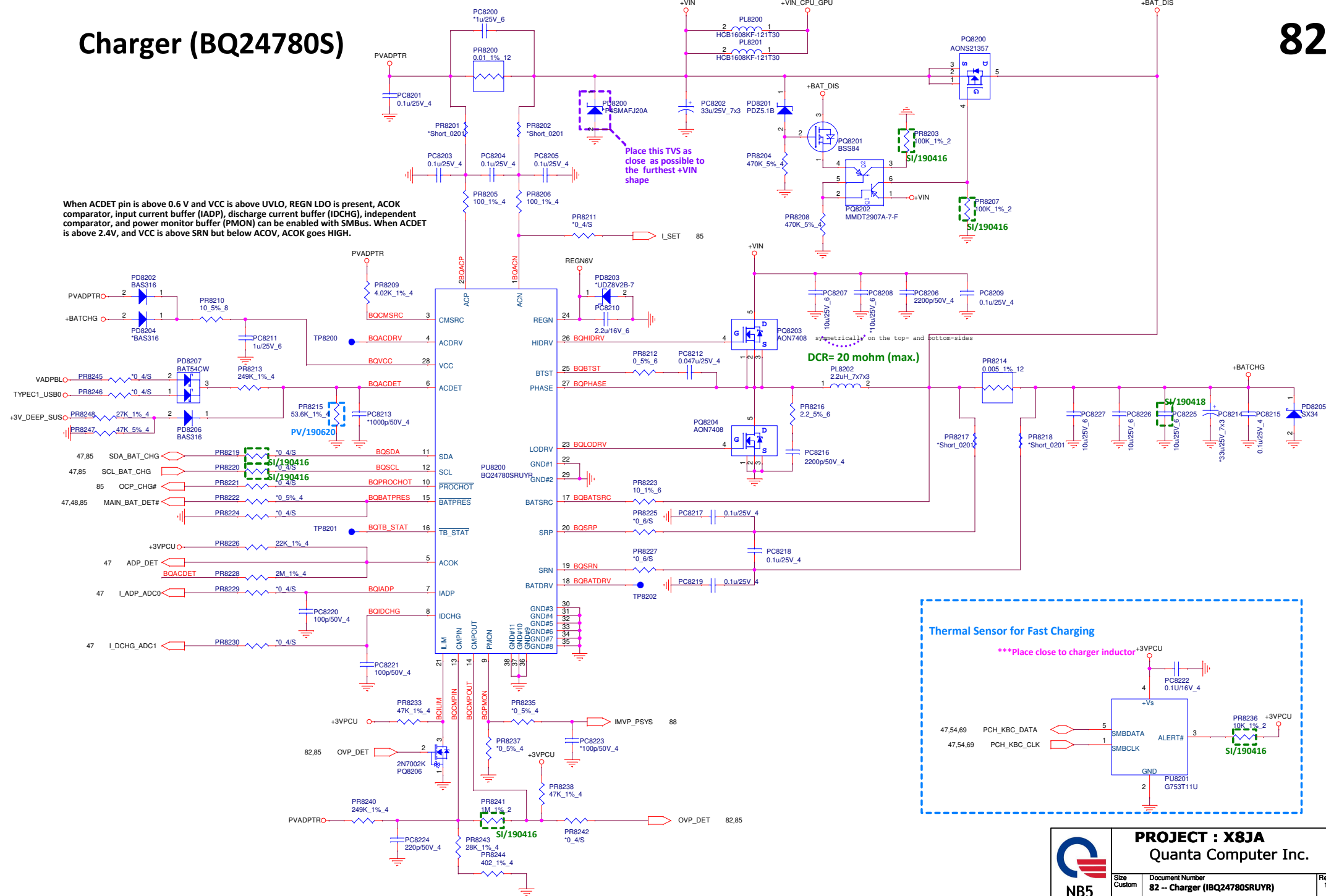





4,5,6,7,9,11,28,29,34,35,36,40,41,43,47,50,51,52,53,54,69,73,76,77,88,95
10,34,35,36,44,50,54,61,73,95
11,33,41,72,73,74,75,85,86,87,93

 NB5	PROJECT : X8JA Quanta Computer Inc.		
	Size Custom	Document Number 81 -- PWROK	Rev 1A
	Date: Thursday, August 15, 2019	Sheet 81	of 106


Charger (BQ24780S)





PROJECT : X8JA
Quanta Computer Inc.

Size Custom	Document Number 83 -- Charger (ISL9538HRTZ-T)	Rev 1A
Date: Thursday, August 15, 2019		Sheet 83 of 106

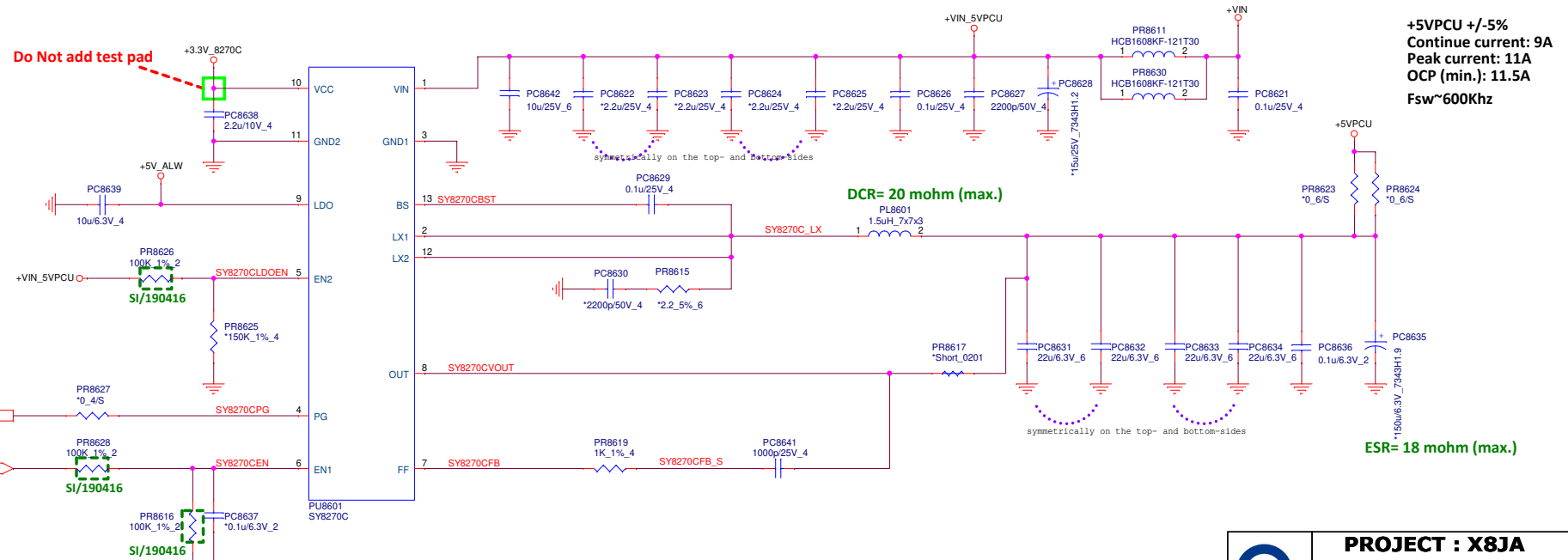
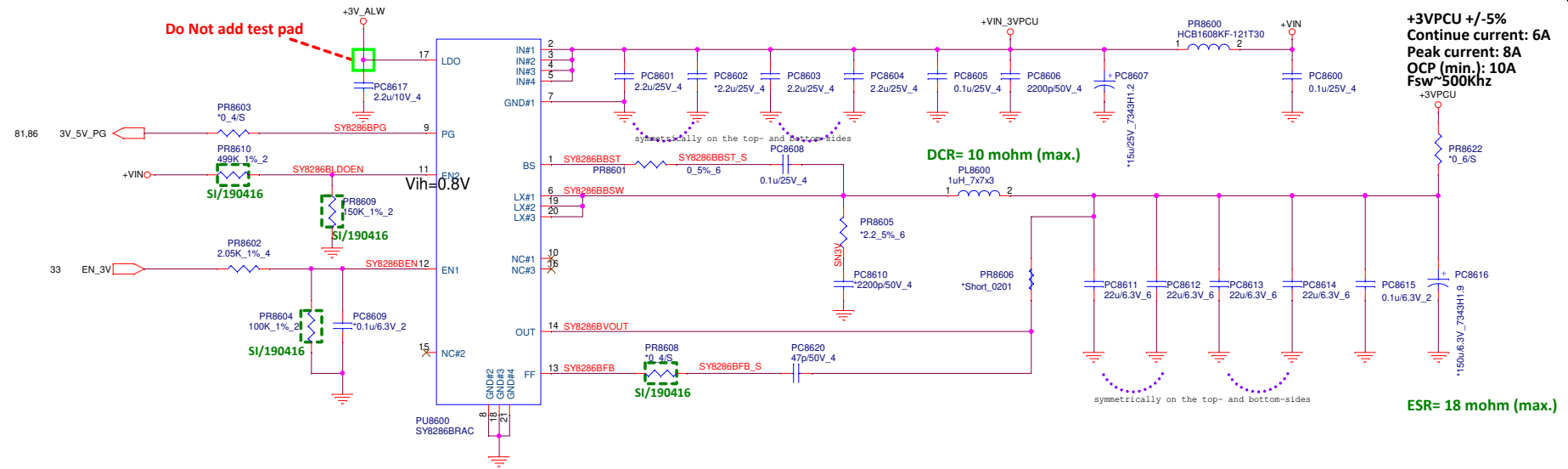


NB5

PROJECT : X8JA
Quanta Computer Inc.

Size Custom	Document Number 84 -- Charger (ISL9538HRTZ-T)	Rev 1A
Date: Thursday, August 15, 2019		Sheet 84 of 106

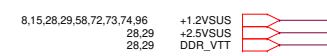


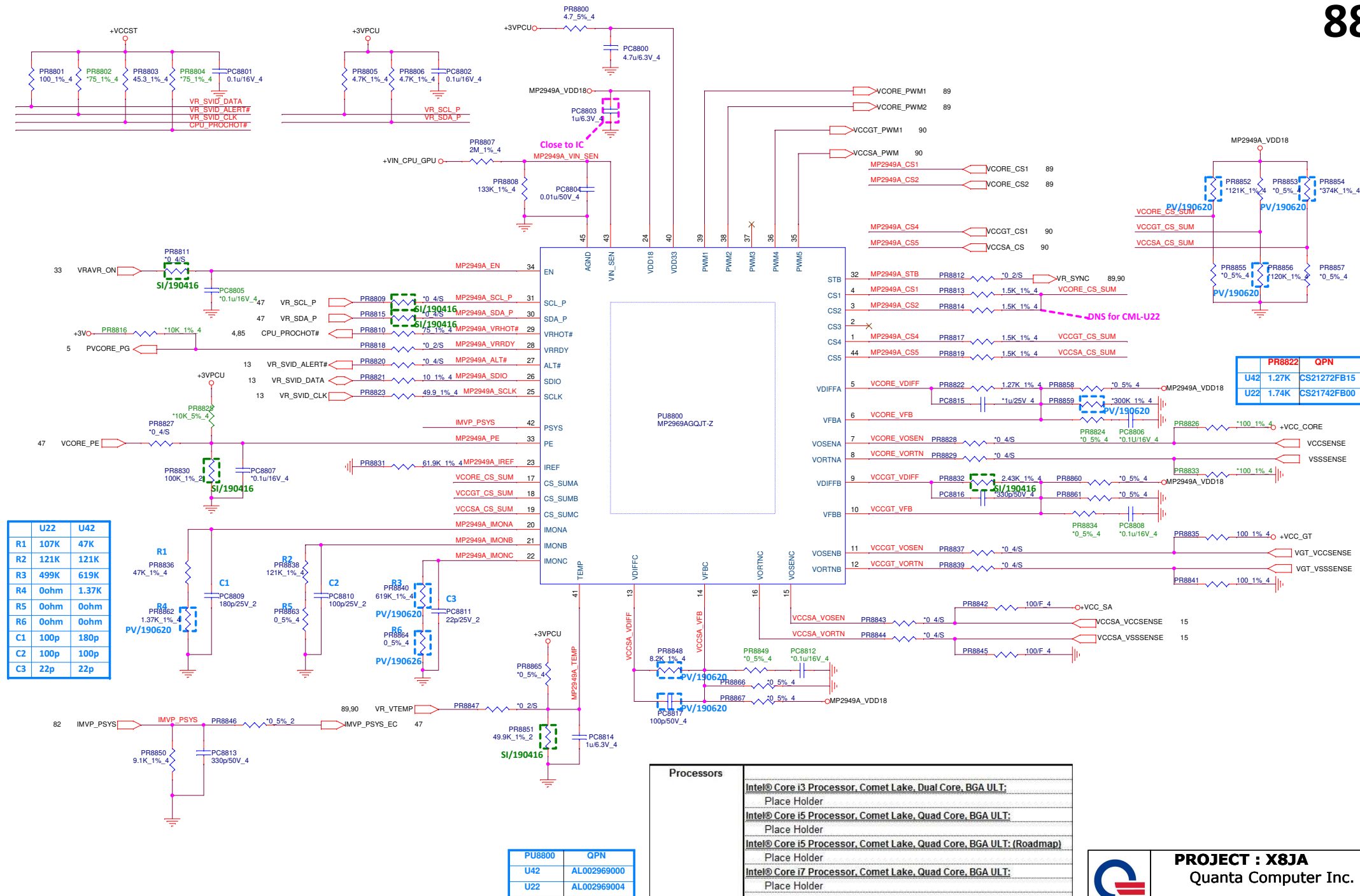


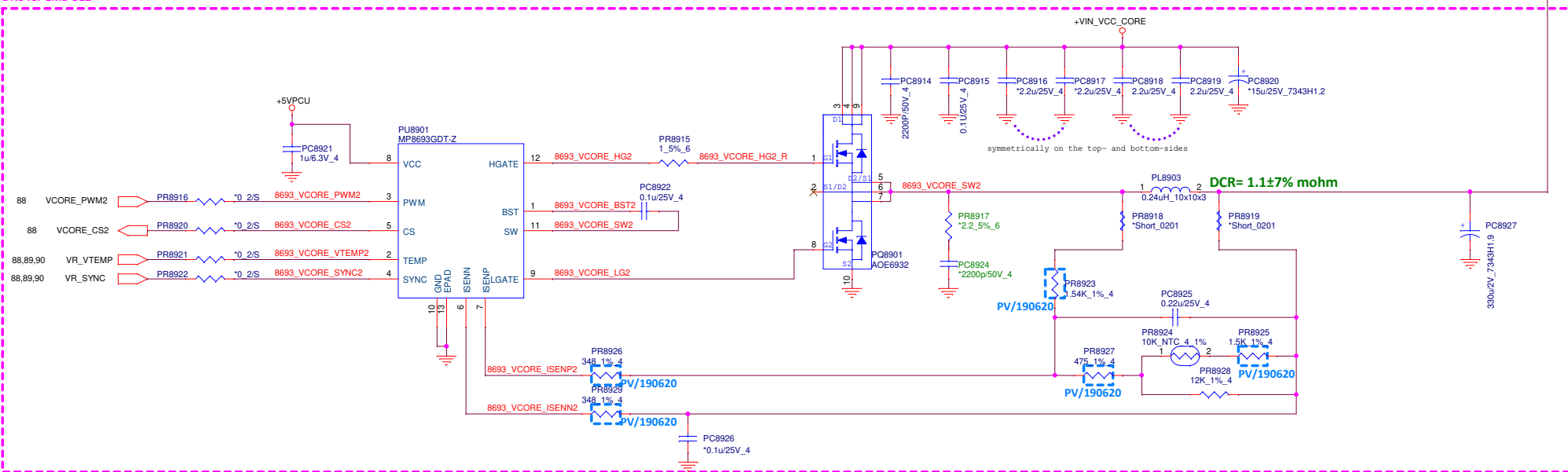
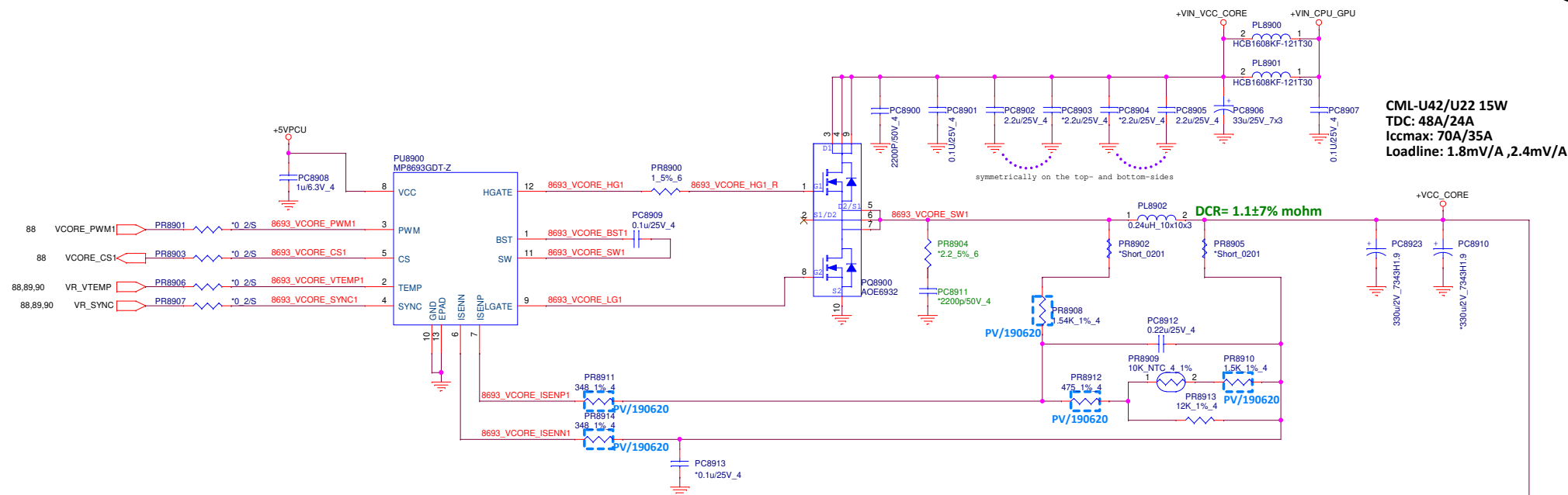
5,7,12,33,34,36,41,42,47,48,50,54,56,58,61,73,74,75,77,80,81,82,85,87,88,92,93,95,105
61,63,72,73,74,76,80,81,87,89,90,92,95,96,98,104,105
72,73,74,81,82,87,93,97

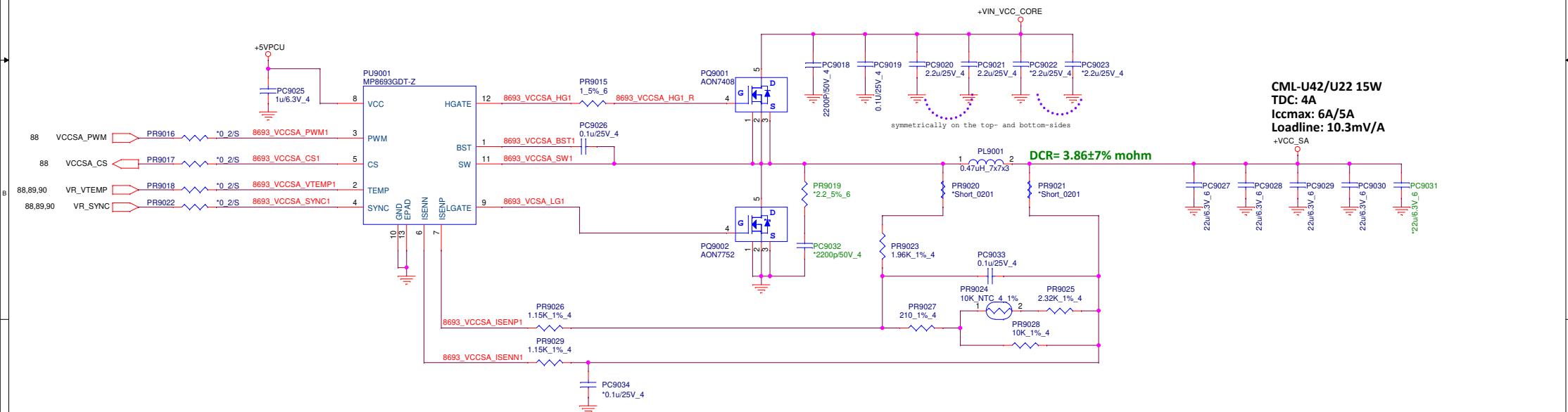
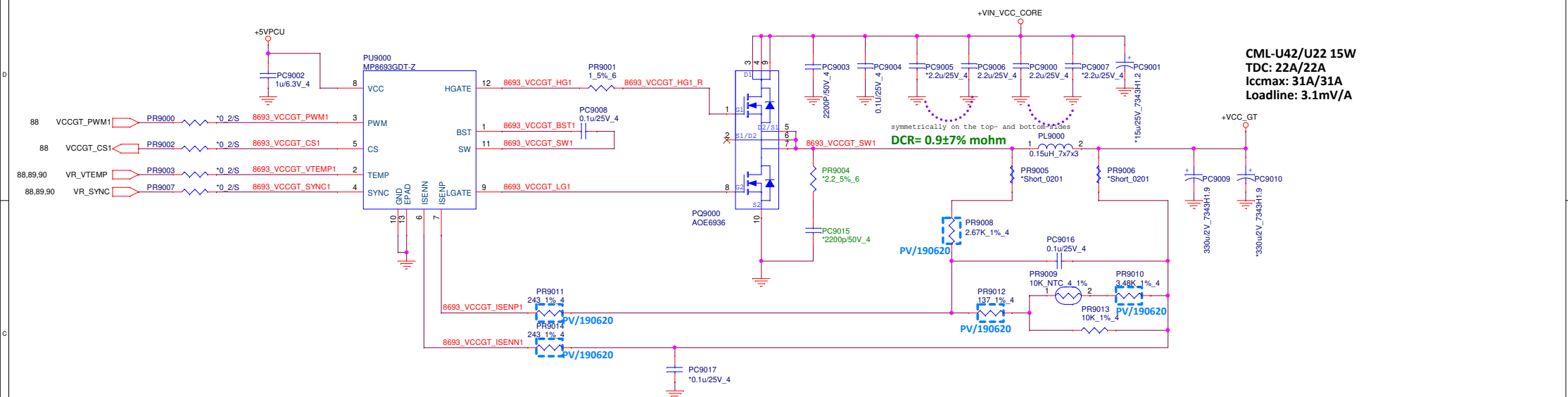
+3VPCU
+5VPCU
+VIN

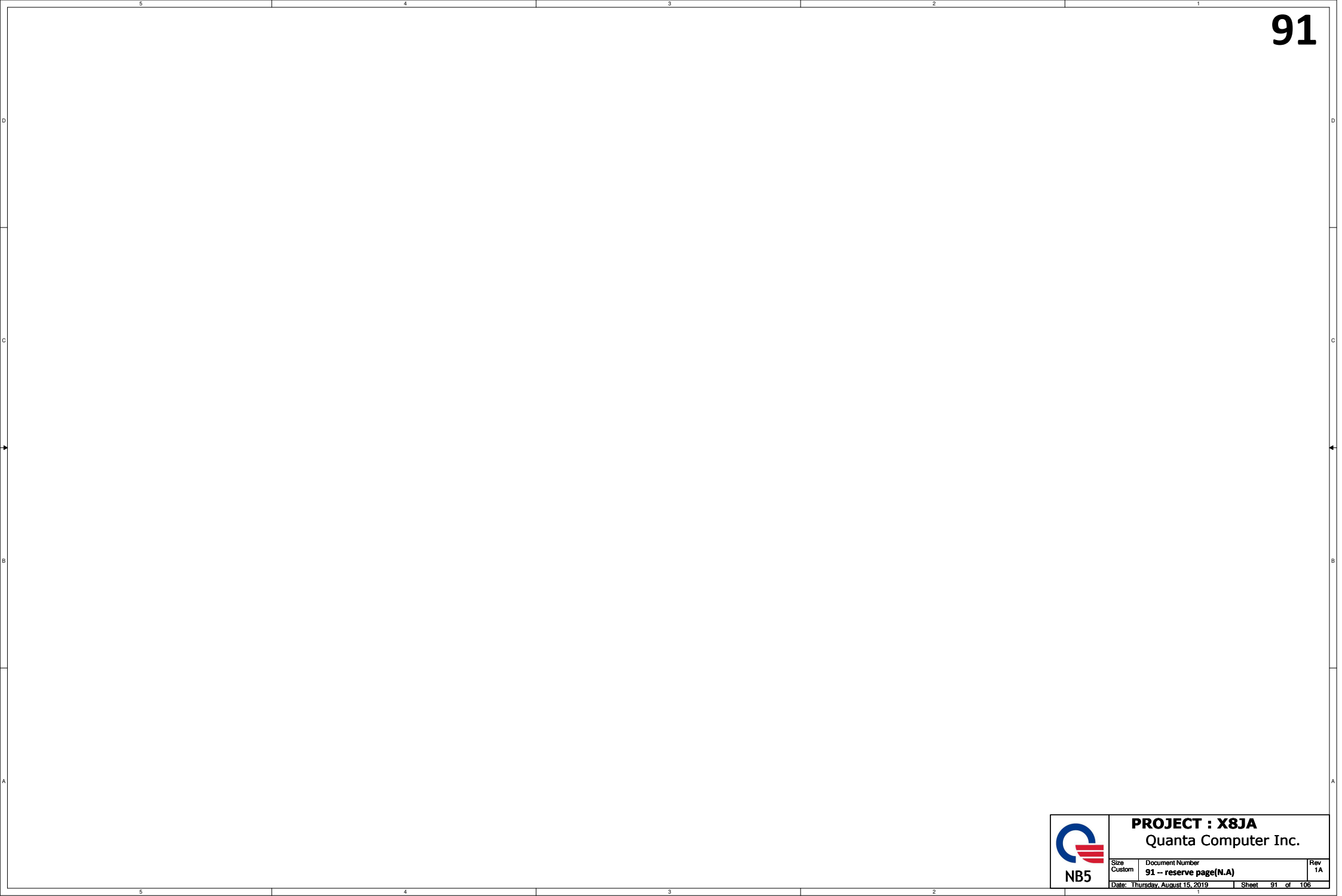
PROJECT : X8JA			
Quanta Computer Inc.			
NB5	Size	Document Number	Rev
	Custom	86 - +3/5V5(SY8286B/SY8286C)	1A
Date: Thursday, August 15, 2019		Sheet 86	of 106








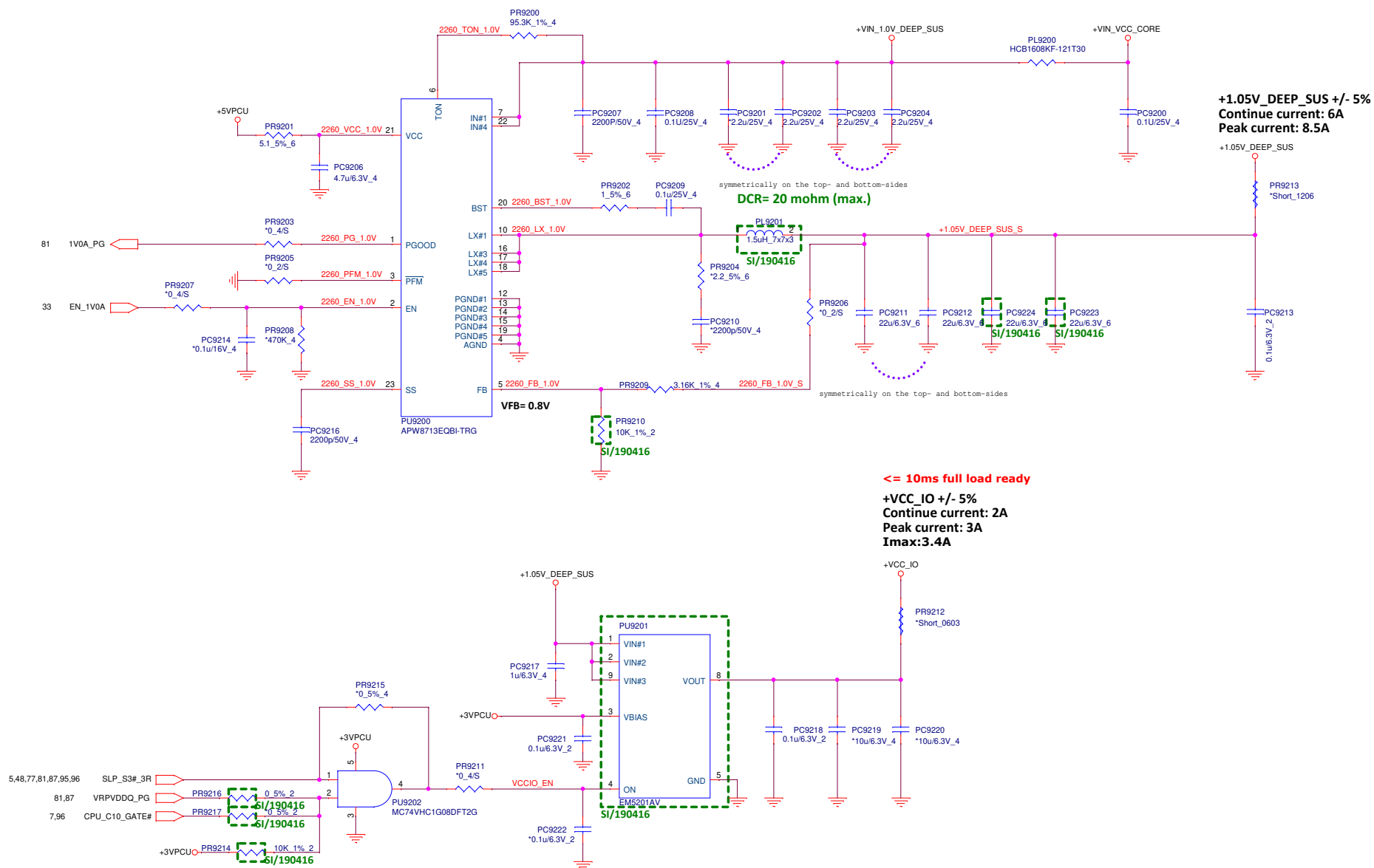






PROJECT : X8JA
Quanta Computer Inc.

Size Custom	Document Number 91 -- reserve page(N.A)	Rev 1A
Date: Thursday, August 15, 2019		Sheet 91 of 106



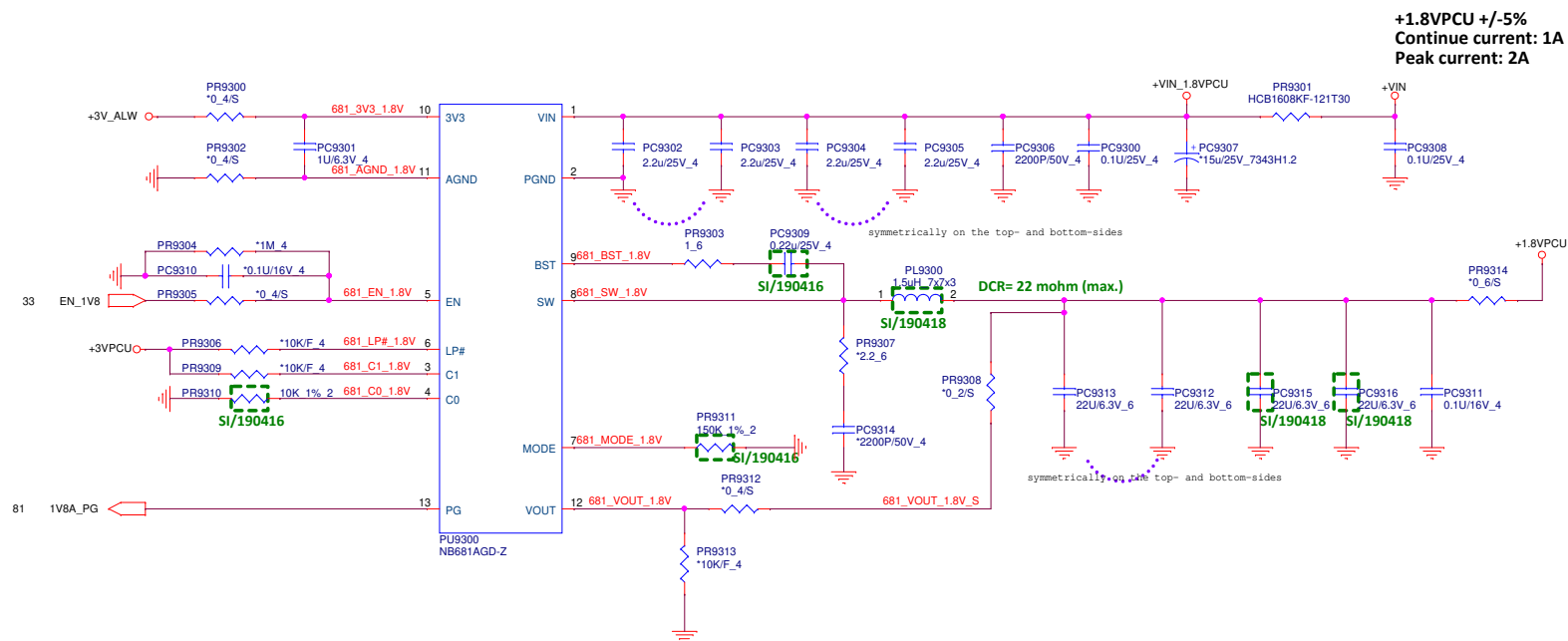
11,12,73,74,77,96

+VCCIO
+1.05V_DEEP_SUS
+1.05V

PROJECT : X8JA
Quanta Computer Inc.

Size	Document Number	Rev
92	92 -- +1.0V_DEEP_SUS(AQZ2260QI)	1A

Date: Thursday, August 15, 2019 Sheet#2 of 106




MODE	VR Rail	Resistor to GND (1% Accuracy)
M1	VCCIO	0
M2	PRIMCORE	Float or > 230K
M3	EDRAM/V1.0A/EOPIO	100K
M4	Others	150K

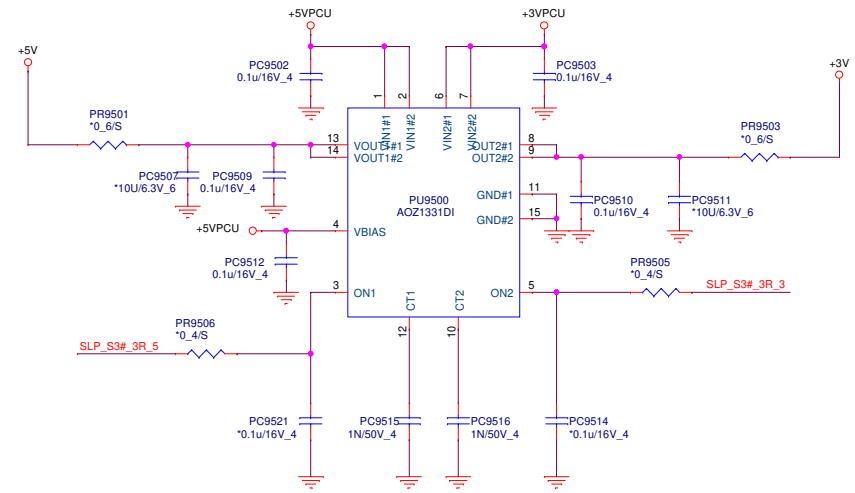
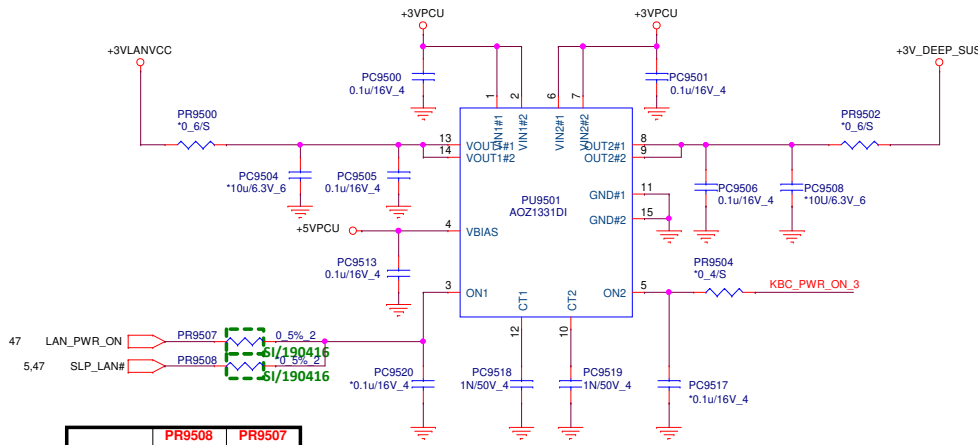
	LP#	C1	C0	VOUT(V)
VCCIO	0	X	X	0
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975
VCCPRIM _CORE	0	X	X	0.7
	1	0	0	0.85
	1	0	1	0.9
	1	1	0	0.95
	1	1	1	1.00
EDRAM/ EOPIO/ V1.0A	0	X	X	0
	1	0	0	0.8 (MSM)
	1	0	1	0.95
	1	1	0	1
	1	1	1	1.05
Others (Fixed design only, not allowed for changing on-the-fly)	0	0	0	1.59
	0	0	1	1.99
	0	1	0	2.38
	0	1	1	3.3
	1	0	0	1.2
	1	0	1	1.5
	1	1	0	1.8
	1	1	1	2.5

Note: LP#, CO and C1 are pulled high internally

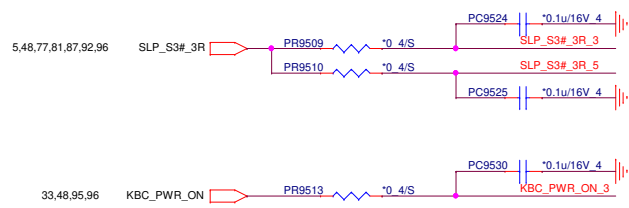
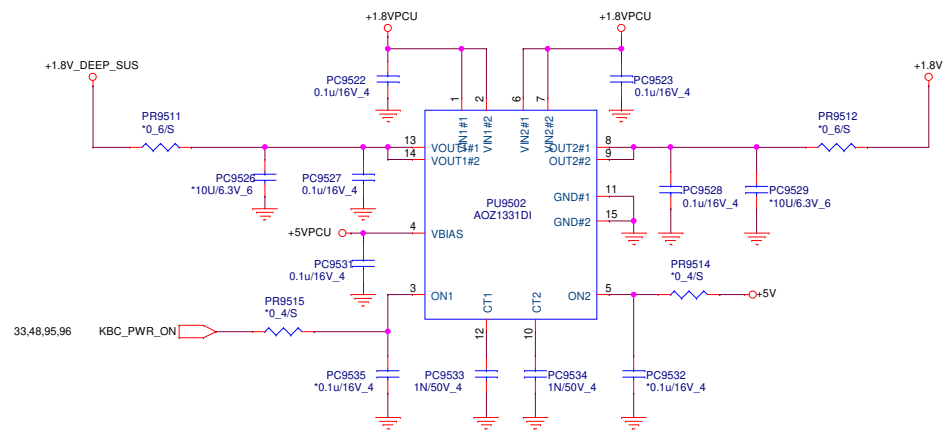
NB5	PROJECT : X8JA Quanta Computer Inc.		
	Size Custom	Document Number 93 -- +1.8VPCU (NB681A)	Rev 1A
	Date: Thursday, August 15, 2019	Sheet 93	of 106



 NB5	PROJECT : X8JA Quanta Computer Inc.		
	Size Custom	Document Number 94 - reserve page	Rev 1A
	Date: Thursday, August 15, 2019 Sheet 94 of 106		



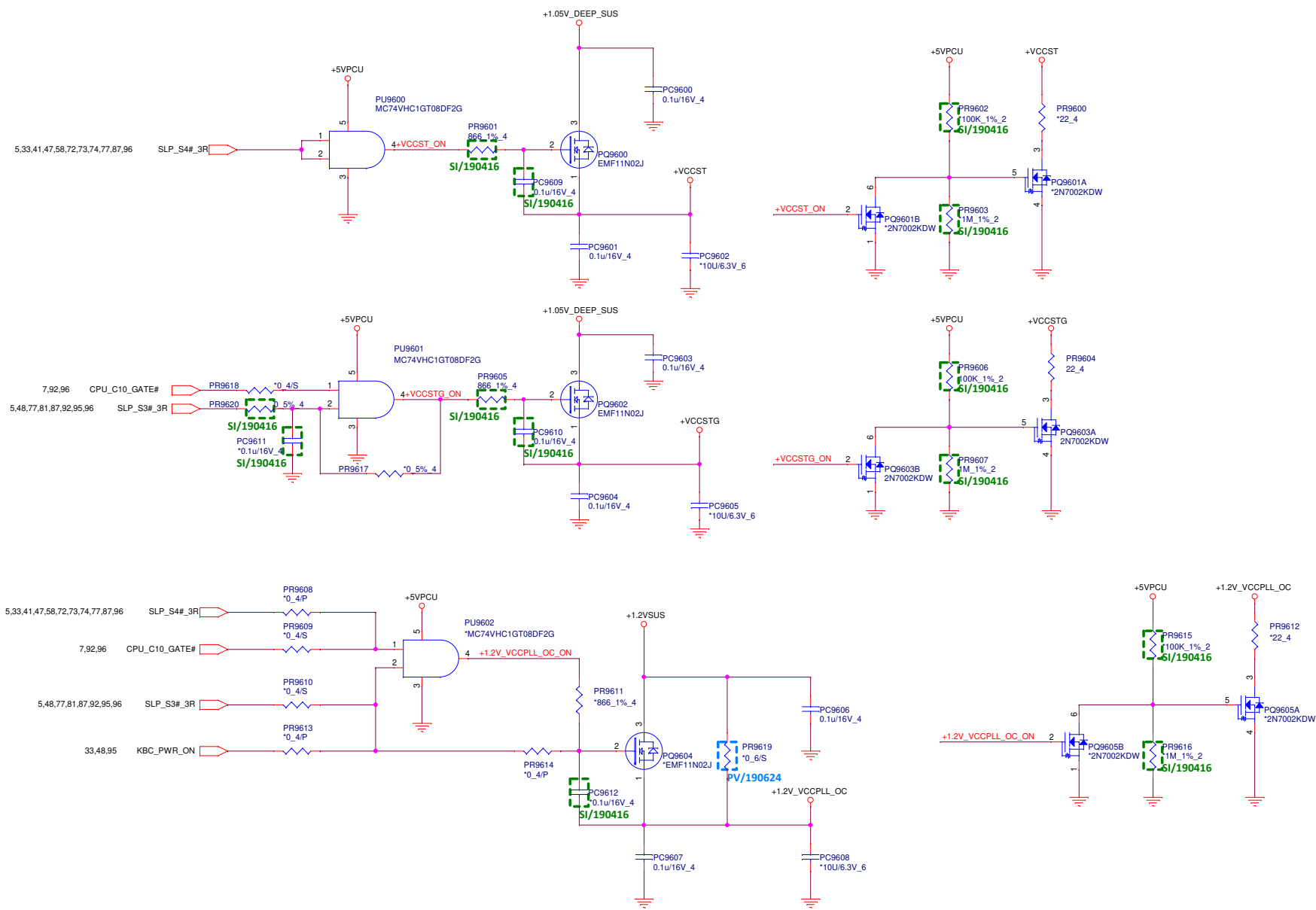
	PR9508	PR9507
VPRO	Staff	Un-staff
Non-Vpro	Un-staff	Staff




- 4,5,6,7,9,11,28,29,34,35,36,40,41,43,47,50,51,52,53,54,69,73,76,77,81,88
- 10,34,35,36,44,50,54,61,73,81
- 72,73,74,81,82,86,87,93,97
- 5,7,12,33,34,36,41,42,47,48,50,54,56,58,61,73,74,75,77,80,81,82,85,86,87,88,92,93,105
- 61,63,72,73,74,76,80,81,86,87,89,90,92,96,98,104,105
- 40
- +3V
- +5V
- +VIN
- +3VPCU
- +5VPCU
- +3VLANVCC

PROJECT : X8JA
Quanta Computer Inc.

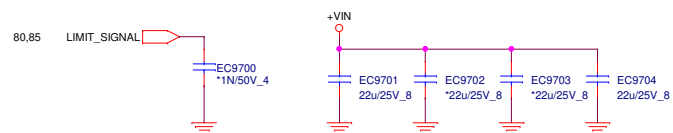
Size Custom	Document Number 95 - Load Switch I (AOZ1331DI)	Rev 1A
Date: Thursday, August 15, 2019		
Sheet	95 of	106



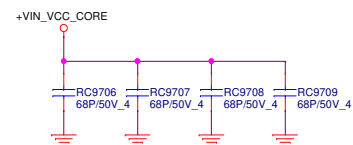
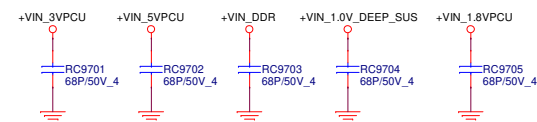
4,5,6,7,9,11,28,29,34,35,36,40,41,43,47,50,51,52,53,54,69,73,76,77,81,88,95
 10,34,35,36,44,50,54,61,73,81,95
 72,73,74,81,82,86,87,93,97
 57,12,33,34,36,41,42,47,48,50,54,56,58,61,73,74,75,77,80,81,82,85,86,87,88,92,93,95,105
 61,63,72,73,74,76,80,81,86,87,89,90,92,95,96,104,105
 40,95

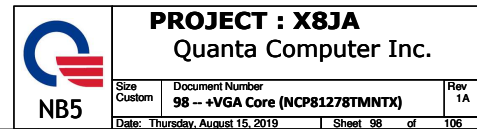
 NB5	PROJECT : X8JA Quanta Computer Inc.		
	Size Custom	Document Number 96 - Load Switch II	Rev 1A
	Date: Thursday, August 15, 2019		Sheet 96 of 106

Reserve for EMI & ISEN test




RF Cap











PROJECT : X8JA
Quanta Computer Inc.

Size Custom	Document Number 99 -- reserve page	Rev 1A
Date: Thursday, August 15, 2019		Sheet 99 of 106



 NB5	PROJECT : X8JA Quanta Computer Inc.		
	Size Custom	Document Number A0 -- reserve page	Rev 1A
	Date: Thursday, August 15, 2019 Sheet 100 of 106		




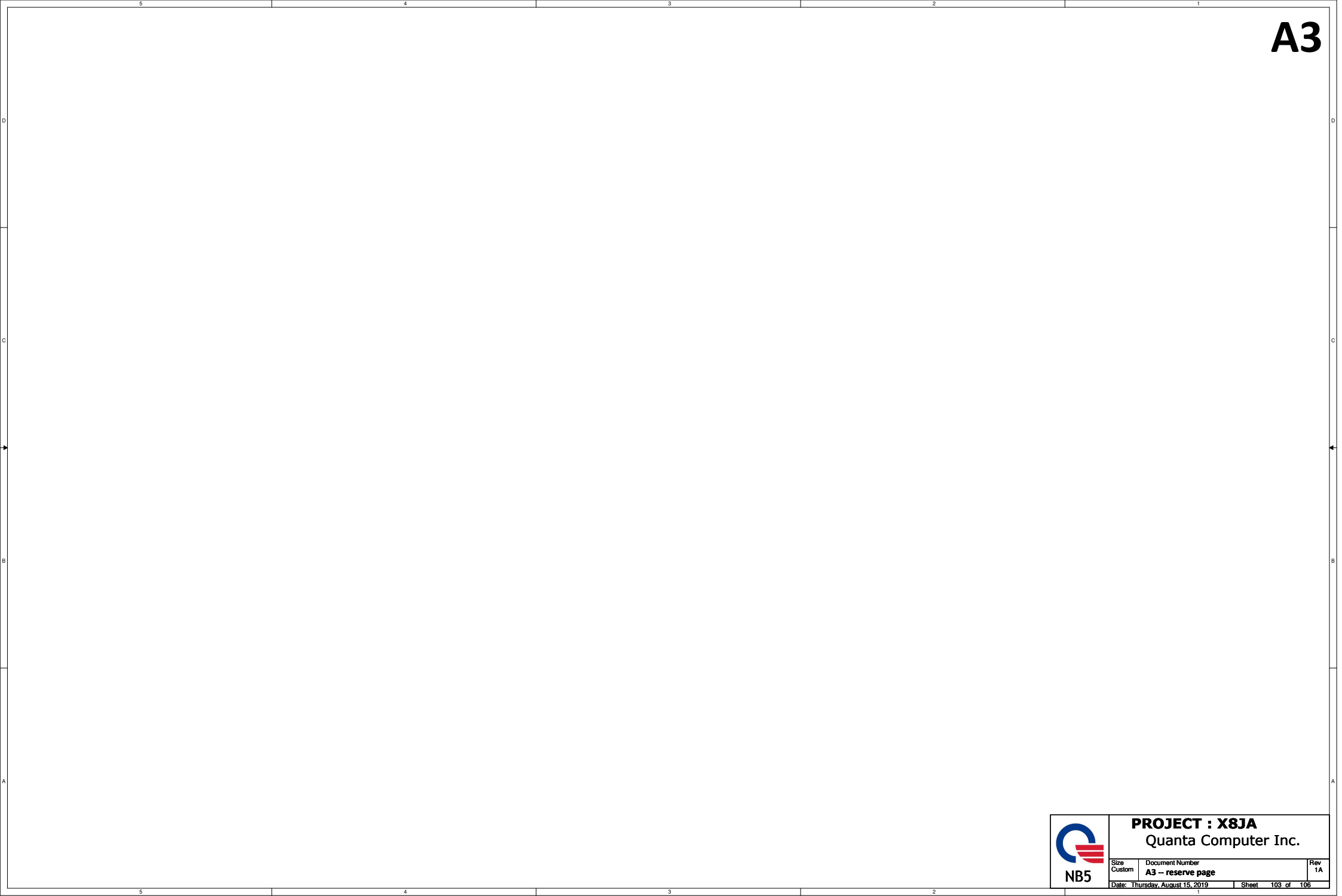
NB5


PROJECT : X8JA
Quanta Computer Inc.

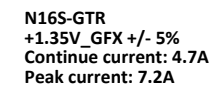
Size Custom	Document Number A1 -- reserve page	Rev 1A
Date: Thursday, August 15, 2019		Sheet 101 of 106



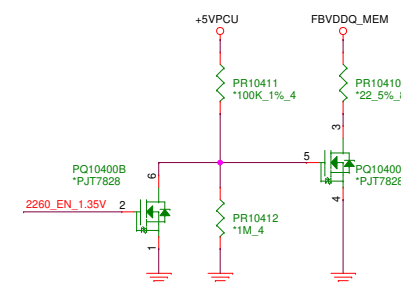
 NB5	PROJECT : X8JA Quanta Computer Inc.		
	Size Custom	Document Number A2 -- reserve page	Rev 1A
	Date: Thursday, August 15, 2019 Sheet 102 of 106		

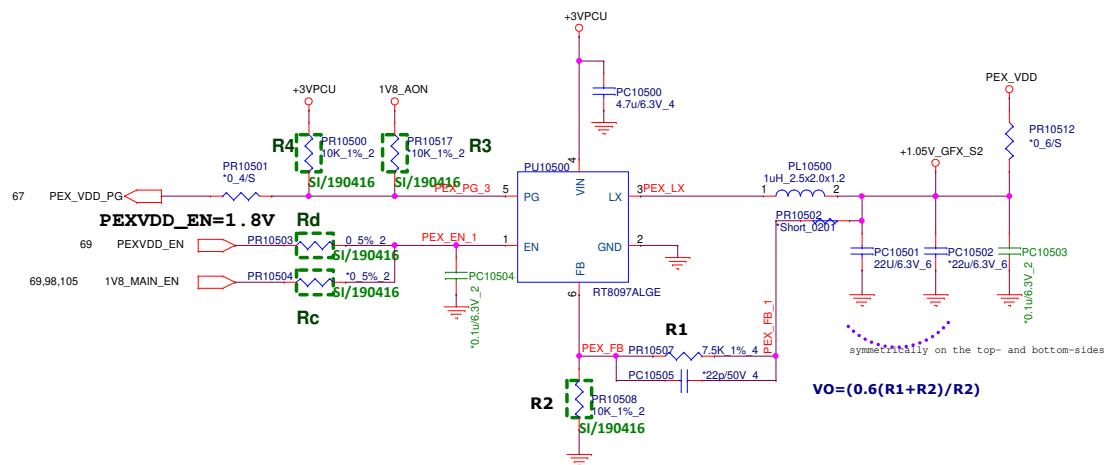


	PROJECT : X8JA Quanta Computer Inc.		
	Size Custom	Document Number A3 -- reserve page	Rev 1A
	Date: Thursday, August 15, 2019 Sheet 103 of 106		



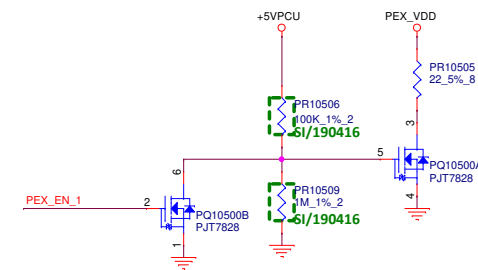
N17S-G1/G2
+1.35V_GFX +/- 5%
Continue current: 5.8A
Peak current: 6.9A



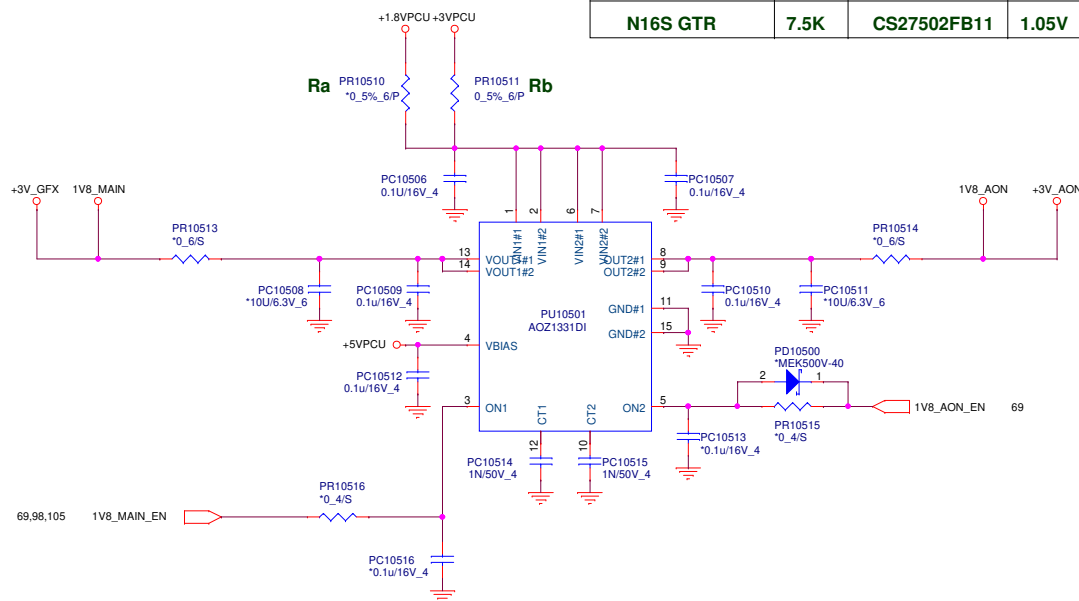


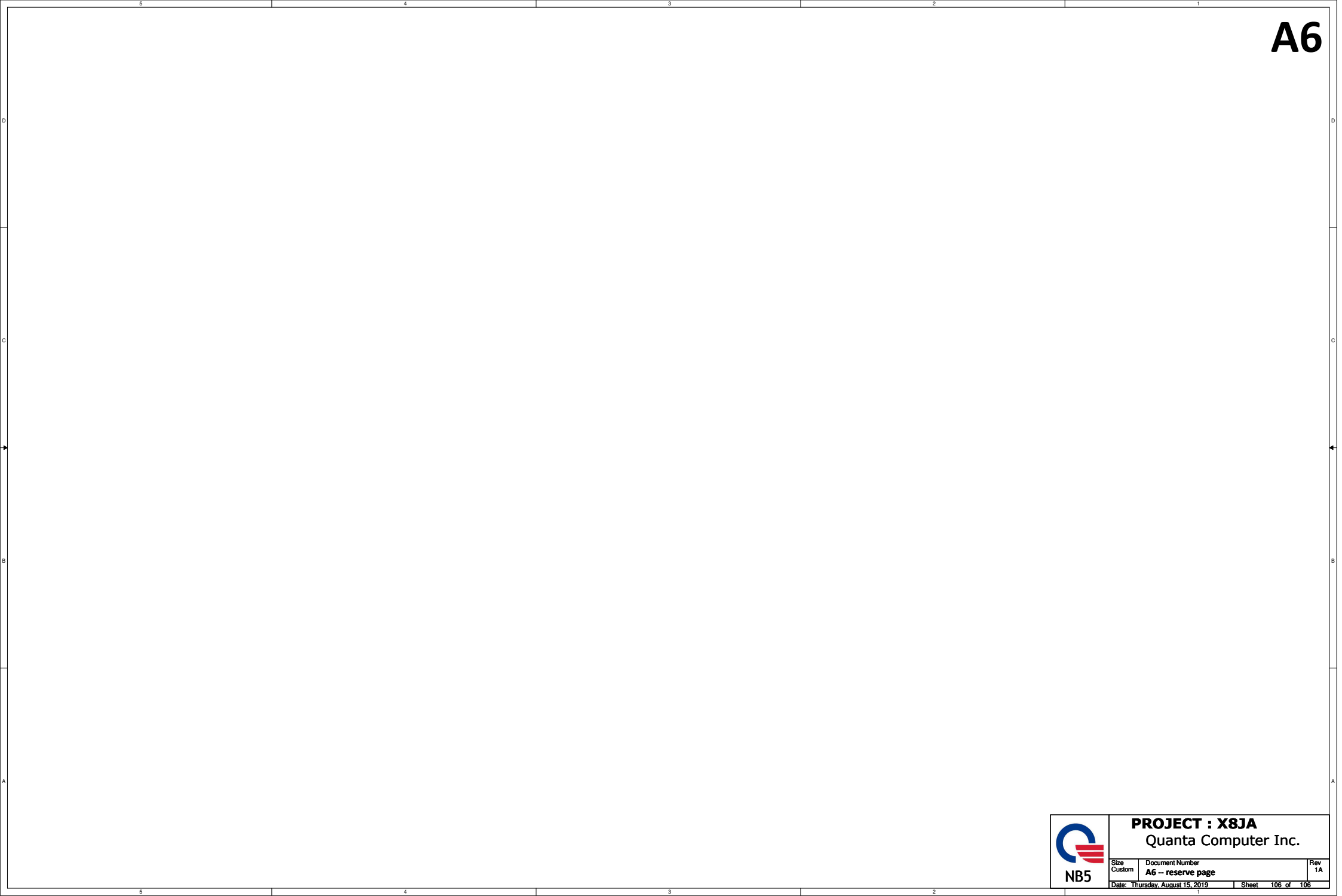
N16S-GTR
+1.05V_GFX +/- 5%
TDC: 0.8A
EDP: 2.1A
OCP: 3.2A


N17S-G1
+1.0V_GFX +/- 5%
TDC: 0.2A
EDP: 0.3A
OCP: 3.2A



	R1	QPN	Vo	R3	R4	Rc	Rd	Ra	Rb
N17S-G1/G2	6.65K	CS26652FB06	1V	Stuff	Unstuff	Unstuff	Stuff	Stuff	Unstuff
N16S GTR	7.5K	CS27502FB11	1.05V	Unstuff	Stuff	Unstuff	Stuff	Unstuff	Stuff





 NB5	PROJECT : X8JA Quanta Computer Inc.		
	Size Custom	Document Number A6 -- reserve page	Rev 1A
	Date: Thursday, August 15, 2019 Sheet 106 of 106		